AC781x Data Sheet

Supports the following：

Part No.	Sub Part No.	Ambient temperature
AC7811xxxx	AC7811QBGE, AC7811OBGE, AC7811MBGE, AC7811QBFE, AC7811OBFE, AC7811MBFE, AC7811JBFE, AC7811QJGE, AC7811OJGE, AC7811MJGE, AC7811OJFE, AC7811MJFE, AC7811JJFE	-40~125°C
AC7813xxxx	AC7813QBGE, AC7813OBGE, AC7813MBGE, AC7813OBFE, AC7813MBFE, AC7813JBFE	-40~85°C
AC7815xxxx	AC7815QBGE, AC7815OBGE, AC7815MBGE, AC7815QBFE, AC7815OBFE, AC7815MBFE, AC7815JBFE	-40~85°C

Version: 1.1

Release date: 2020-01-03

Document Revision History

Revision	Date	Author	Description
1.0	2019-02-19	AutoChips	Initial Version
1.1	2020-01-03	AutoChips	Add 85° and 105° power consumption data

Table of Contents

1 Key Features

- Operating characteristics
  - Voltage range: 2.7 to 5.5 V
  - Temperature range (ambient): -40 to 125°C
- Performance
  - Up to 100 MHz ARM® Cortex-M3 core
  - Single cycle 32-bit x 32-bit multiplier
  - Fast I/O access port
- Memories and memory interfaces
  - Up to 256 KB flash
  - Up to 64 KB RAM
- Clocks
  - Oscillator (OSC) - supports 4 MHz to 30 MHz crystal or ceramic resonator; choice of low power or high gain oscillators
  - Internal clock source (ICS) - internal PLL with internal or external reference, 8 MHz pre-trimmed internal reference for 100 MHz system clock
  - Internal 32 kHz low-power oscillator (LPO)
- System peripherals
  - Power management module (PMC) with three power modes: Run, Wait, Stop
  - Low-voltage detection (LVD) with reset
  - Watchdog with independent clock source(WDOG)
  - Programmable cyclic redundancy check module(CRC)
  - Serial wire debug (SWD) & JTAG interfaces
  - Cortex®-M3 Embedded Trace Macrocell™
  - Aliased SRAM bitband region (BIT-BAND)
  - One 12-channel DMA
- Human-machine interface
  - Up to 68 general-purpose input/output (GPIO)
  - External interrupt (IRQ)
- Analog modules
  - One up to 16-channel 12-bit SAR ADC, operation in Stop mode, optional hardware trigger (ADC)
  - Two analog comparators containing a 6-bit DAC and programmable reference input(ACMP)
- Timers
  - One 6-channel PWM
  - Three 2-channel PWM
  - One 8-channel periodic interrupt timer (TIMER)
  - One pulse width timer (PWDT)
  - One real-time clock (RTC)
- Communication interfaces
  - Two SPI modules (SPI)
  - Up to SIX UART modules (one support Software LIN)
  - Two I2C modules (I2C)
  - Two CAN module (CAN)
  - One Hardware Lin module(LIN)
- Package options
  - 80-pin LQFP
  - 64-pin LQFP

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:
AC## GTUFPN

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Table 1. Fields

Field	Description	Values
AC##	ATC mcu family	• AC78
G	Generation	• 1= the first generation
T	Temperature range (°C)	• 1= AEC-Q100 Grade 1 • 3= AEC-Q100 Grade 3 • 5= 85°C
U	User flash memory size	• Q = 256 KB • O = 128 KB • M = 64 KB • J = 32 KB
F	Grade definition	• B = Normal Grade • J = BCM Grade
P	Package identifier	• F = 64 (7 mm x 7 mm) • G = 80 (10 mm x 10 mm)
N	Packaging type	• E = LQFP

2.4 Example

This is an example part number: AC7811QBGE.

3 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods.To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 2. Parameter classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

4 Ratings

4.1 Thermal handling ratings

Table 3. Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, High Temperature Storage Life.
2. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

4.2 Moisture handling ratings

Table 4. Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

4.3 ESD handling ratings

Table 5. ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	–8000	8000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	–750	750	V	2
I_{LAT}	Latch-up current at ambient temperature of 125°C	–200	200	mA	3

1.Determined according to AEC-Q100-002-D,HUMAN BODY MODEL ELECTROSTATIC DISCHARGE TEST.
2.Determined according to AEC-Q100-011-C1,CHARGED DEVICE MODEL (CDM) ELECTROSTATIC DISCHARGE TEST.
3. Determined according to AEC-Q100-004-D,IC LATCH-UP TEST.

- Test was performed at 125 °C case temperature (Class II).
- Supply groups pass 1.5 Vccmax.

4.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in the following table may affect device reliability or cause

permanent damage to the device. For functional operating conditions, refer to the remaining tables in this document.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either VSS or VDD) or the programmable pullup resistor associated with the pin is enabled.

Table 6. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	6	V
I_{DD}	Maximum current into V_{DD}	—	60	mA
V_{IN}	Input voltage except true open drain pins	–0.3	V_{DD} + 0.3[1]	V
	Input voltage of true open drain pins	–0.3	V_{DD} + 0.3[1]	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–20	20	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V

1. Maximum rating of VDD also applies to VIN.

5 General

5.1 Nonswitching electrical specifications

5.1.1 Power and ground pins

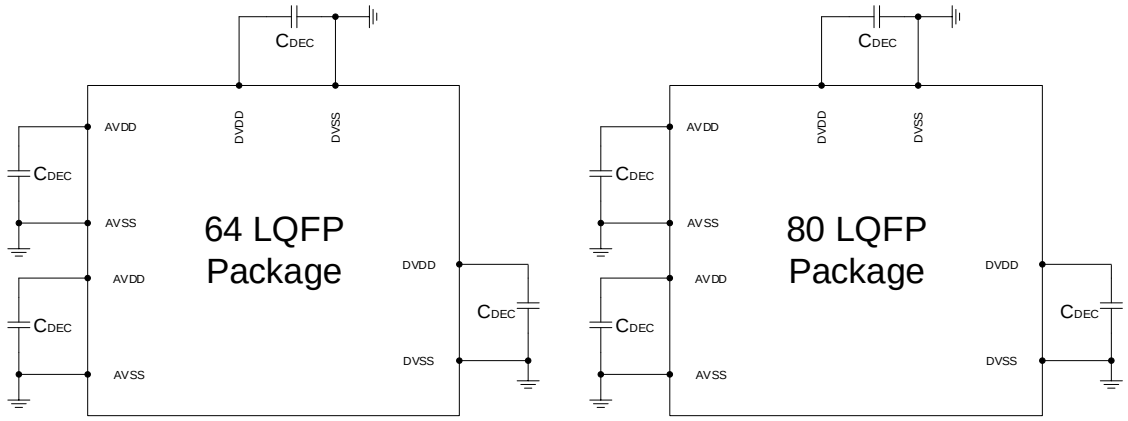

Figure 1. Pinout decoupling

1. DVDD and AVDD must be shorted to a common source on PCB.
2. All decoupling capacitors must be low ESR ceramic capacitors (X7R type) , the recommended value is 0.1 uF.
3. For improved performance, it is recommended to use 10 uF,0.1 uF and 1 nF capacitors in parallel.
4. All decoupling capacitors should be placed as close as possible to the corresponding power and ground pins.

5.1.2 DC characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 7. DC characteristics

Symbol	C	Descriptions			Min	Typical	Max	Unit
—	—	Operating voltage		—	2.7	—	5.5	V
V_{OH}	P	Output high voltage	drive strength	5 V, I_{load} = -5, -10, -15, -20mA	0.85×V_{DD}	—	—	V
	C			3 V, I_{load} = –3.6, -7.2,-10.8,-14.4 mA	0.8×V_{DD}	—	—	V
I_{OHT}	D	Output high current	Max total I_{OH} for all ports	5 V	—	—	30	mA
				3 V	—	—	20	
V_{OL}	P	Output low voltage	drive strength	5 V, I_{load} = 5, 10, 15, 20mA	—	—	0.15×V_{DD}	V

	C			3 V, I_{load} = 3.6, 7.2,10.8,14.4 mA	—	—	0.2×V_{DD}	V
I_{OLT}	D	Output low current	Max total I_{OL} for all ports	5 V	—	—	30	mA
				3 V	—	—	20	
V_{IH}	P	Input high voltage	All digital inputs	4.5≤V_{DD}<5.5 V	0.65 × V_{DD}	—	V_{DD} + 0.3	V
				2.7≤V_{DD}<4.5 V	0.70 × V_{DD}	—	V_{DD} + 0.3	
V_{IL}	P	Input low voltage	All digital inputs	4.5≤V_{DD}<5.5 V	-0.3	—	0.35 × V_{DD}	V
				2.7≤V_{DD}<4.5 V	-0.3	—	0.30 × V_{DD}	
V_{hys}	C	Input hysteresi s	All digital inputs	—	0.06 × V_{DD}	—	—	mV
$\|I_{In}\|$	P	Input leakage current	Per pin (pins in high impedance input mode)	V_{IN} = V_{DD} or V_{SS}	-1	0.1	1	µA
$\|I_{INTOT}\|$	C	Total leakage combine d for all port pins	Pins in high impedance input mode	V_{IN} = V_{DD} or V_{SS}	0	0.1	2	µA
R_{PU}	P	Pullup resistors	All digital inputs, when enabled	—	40	75	90	kΩ
I_{IC}	D	DC injection current[4,5,6]	Single pin limit	V_{IN} < V_{SS}, V_{IN} > V_{DD}	-2	—	2	mA
			Total MCU limit, includes sum of all stressed pins		-5	—	25	
C_{In}	C	Input capacitance, all pins		—	—	5	7	pF
V_{RAM}	C	RAM retention voltage		—	2	—	—	V

Table 8. LVD /POR / AVDD Voltage warning specification

Symbol	C	Description	Min	Typical	Max	Unit
V_{POR}	D	POR re-arm voltage[1]	1.6	1.8	2	V
V_{LVDL}	C	Falling low-voltage detect threshold—low range (LVDV= 0)	2.5	2.55	2.6	V
V_{LVDH}	C	Falling low-voltage detect threshold—high range (LVDV=1)[2]	4.1	4.2	4.3	V

V_{HYSLVD}	C	low-voltage detect hysteresis		—	50	—	mV
V_{LVW1H}	C	Falling low-voltage warning threshold— high range	Level 1 falling(LVWV = 00)	4.2	4.3	4.4	V
V_{LVW2H}	C		Level 2 falling(LVWV = 01)	4.3	4.4	4.5	V
V_{LVW3H}	C		Level 3 falling(LVWV = 10)	4.4	4.5	4.6	V
V_{LVW4H}	C		Level 4 falling(LVWV = 11)	4.5	4.6	4.7	V
V_{LVW1L}	C	Falling low-voltage warning threshold— low range	Level 1 falling(LVWV = 00)	2.5	2.6	2.7	V
V_{LVW2L}	C		Level 2 falling(LVWV = 01)	2.6	2.7	2.8	V
V_{LVW3L}	C		Level 3 falling(LVWV = 10)	2.7	2.8	2.9	V
V_{LVW4L}	C		Level 4 falling(LVWV = 11)	2.8	2.9	3	V
V_{HYSPVD}	C	Program low-voltage detect hysteresis		—	50	—	mV
V_{BG}	P	Buffered bandgap output [3]		1.19	1.2	1.21	V

1. Maximum is highest voltage that POR is guaranteed.
2. Rising thresholds are falling threshold + hysteresis.
3. voltage Factory trimmed at VDD = 5.0 V, Temp = 25 °C

5.1.3 Supply current characteristics

Table 9. Supply current characteristics

Parameter	Symbol	Core/BusFreq	V_{DD} (V)	25° [1]	85°	105°	125° [2]	Unit
LFOSC+PLL, all modules clocks enabled;	RI_{DD}	96/48 MHz	5	18.55	18.72	18.859	18.91	mA
		48/48 MHz		13.32	13.526	13.596	13.612	
		12/12 MHz		7.55	7.616	7.641	7.742	
		96/48 MHz	3.3	18.091	18.267	18.289	18.313	
		48/48 MHz		12.892	12.895	13.013	13.073	
		12/12 MHz		7.182	7.192	7.21	7.256	
LFOSC+PLL, all modules clocks disabled and gated;	RI_{DD}	96/48 MHz	5	15.996	16.544	16.696	16.858	mA
		48/48 MHz		11.147	11.855	11.814	12.054	
		12/12 MHz		6.206	6.676	6.787	6.918	
		96/48 MHz	3.3	15.711	16.006	16.119	16.286	
		48/48 MHz		10.912	11.138	11.284	11.543	
		12/12 MHz		6.015	6.159	6.292	6.413	
XOSC+PLL, all modules clocks enabled;	RI_{DD}	96/48 MHz	5	21.537	21.899	21.946	22.214	mA
		48/48 MHz		16.299	16.521	16.585	16.947	
		12/12 MHz		10.079	10.583	10.629	11.12	
		96/48 MHz	3.3	21.021	21.029	21.307	21.568	
		48/48 MHz		15.823	15.708	15.993	16.338	
		12/12 MHz		10.101	9.805	10.083	10.558	
XOSC+PLL, all modules clocks disabled and gated;	RI_{DD}	96/48 MHz	5	18.97	20.07	20.12	20.794	mA
		48/48 MHz		14.136	15.286	15.301	15.345	
		12/12 MHz		9.178	10.229	10.237	10.286	
		96/48 MHz	3.3	18.639	19.209	19.509	20.097	
		48/48 MHz		13.847	14.472	14.659	14.706	
		12/12 MHz		8.934	9.447	9.537	9.698	
Sleep mode LFOSC+PLL, all modules clocks enabled	WI_{DD}	96/48 MHz	5	14.91	15.441	15.64	15.695	mA
		48/48 MHz		10.638	11.197	11.305	11.384	

		12/12 MHz		6.088	6.564	6.658	6.762	
		96/48 MHz	3.3	14.635	14.952	15.095	15.105	
		48/48 MHz		10.404	10.642	10.795	10.834	
		12/12 MHz		5.891	6.048	6.188	6.252	
Sleep mode XOSC+PLL, all modules clocks enabled	WIDD	96/48 MHz	5	17.934	18.824	18.954	19.07	mA
		48/48 MHz		13.664	14.578	14.625	14.786	
		12/12 MHz		9.103	10.043	10.078	10.185	
		96/48 MHz	3.3	17.614	18.286	18.349	18.404	
		48/48 MHz		13.379	13.978	14.066	14.167	
		12/12 MHz		8.859	9.369	9.553	9.603	
Stop mode (RTC/GPIO/I2C/SPI/UART/ CAN/LIN can wake up) 3	SIDD	—	5	5.2	61.62	130	132.29	µA
		—	3.3	5	60.36	128.32	129.05	
Standby mode(RTC on, RTC/NMI can wake up) 3	SIDD	—	5	2.1	15.62	30.68	33.47	µA
		—	3.3	2	13.75	28.63	30.46	
ADC adder to Stop mode	—	—	5	85	TBD	TBD	212.09	µA
			3.3	78	TBD	TBD	202.05	
ACMP adder to Stop mode	—	—	5	6.1	TBD	TBD	37.47	µA
			3.3	6	TBD	TBD	34.46	
LVD adder to Stop mode	—	—	5	50.5	86.03	156.41	156.7	µA
			3.3	45.8	83.81	151.77	152.5	

1. Data in Typical column was characterized at 3.3/5.0 V, 25 °C or is typical recommended value.
2. Data in Typical column was characterized at 3.3/5.0 V, 125 °C or is typical recommended value.
3. RTC adder cause <1 µA IDD increase typically, RTC clock source is 32 kHz LPO clock.

5.2 Switching specifications

5.2.1 Control timing

Table 10. Control timing

Num	C	Rating		Symbol	Min	Typical[1]	Max	Unit
1	D	System and core clock (t_{sys} = 1/f_{Sys})		f_{Sys}	DC	—	100	MHz
2	P	Bus frequency (t_{cyc} = 1/f_{Bus})		f_{Bus}	DC	—	50	MHz
3	P	Internal low power oscillator frequency		f_{LPO}		32		KHz
4	D	External reset pulse width2		t_{extrst}	1.5 × t_{32k}	—	—	ns
5	D	IRQ pulse width	Run mode3	t_{ILIH}/ t_{IHIL}	1.5 × t_{sys}	—	—	ns

	D		Stop mode[3]	t_{ILIH}/ t_{IHIL}	1.5 × t_{32k}	—	—	ns
6	C	Port rise and fall time - Normal drive strength(load = 50 pF)[4]	—	t_{Rise}	—	10.2	—	ns
	C			t_{Fall}	—	9.5	—	ns
	C	Port rise and fall time - high drive strength(load = 50 pF)[4]	—	t_{Rise}	—	5.4	—	ns
	C			t_{Fall}	—	4.6	—	ns

1. Typical values are based on characterization data at VDD = 5.0 V, 25 °C unless otherwise stated.
2. This is the shortest pulse that is guaranteed to be recognized as a RESET pin request.
3. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized.
4. Timing is shown with respect to 20% VDD and 80% VDD levels. Temperature range -40 °C to 125 °C.

5.2.2 PWM module timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the PWM clock.

Table 11. PWM input timing

C	Function	Symbol	Min	Max	Unit
D	Timer clock frequency	f_{PWM}	-	48M	Hz
D	External clock frequency	f_{Tclk}	0	f_{PWMr}/4	Hz
D	External clock period	t_{Tclk}	4	—	t_{PWM}[1]
D	External clock high time	t_{clkh}	1.5	—	t_{PWM}
D	External clock low time	t_{clkl}	1.5	—	t_{PWM}
D	Input capture pulse width	t_{ICPW}	1.5	—	t_{PWM}

1. $t_{PWM}=1/f_{PWM}$.

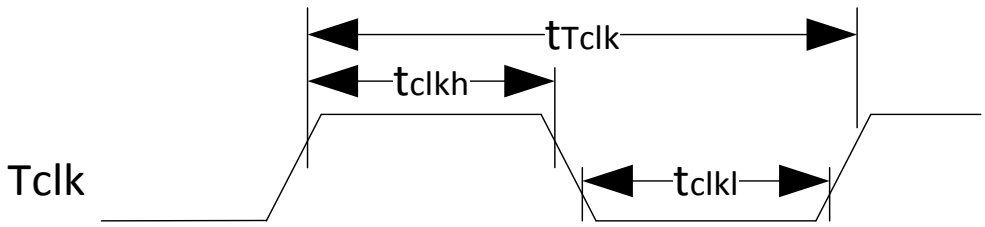

Figure 2. Timer external clock

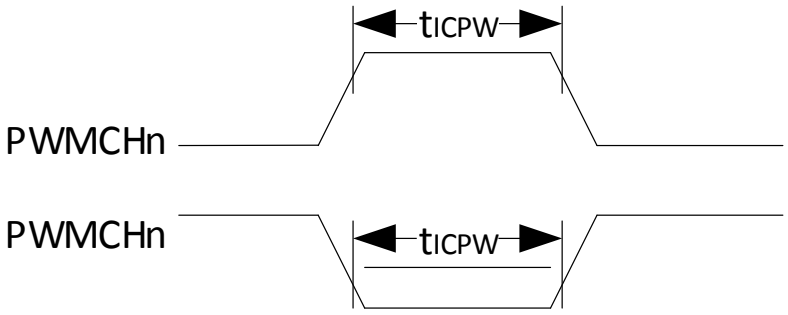

Figure 3. Timer input capture pulse

5.3 Thermal specifications

5.3.1 Thermal characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user- determined rather than being controlled by the MCU design. To take PI/O into account in power calculations, determine the difference between actual pin voltage and VSS or VDD and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and VSS or VDD will be very small.

Table 12. Thermal characteristics

Board type	Symbol	Description	64 LQFP	80 LQFP	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	71	57	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	53	44	°C/W	1, 3
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	59	47	°C/W	1, 3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	46	38	°C/W	1, 3
—	$R_{\theta JB}$	Thermal resistance, junction to board	35	28	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	20	15	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center(natural convection)	5	3	°C/W	6

The average chip-junction temperature (T_J) in °C can be obtained from:

$T_J = T_A + (P_D \times \theta_{JA})$ Where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts - chip internal power

$P_{I/O}$ = Power dissipation on input and output pins - user determined
For most applications, $P_{I/O}$ << P_{int} and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:
$P_D = K \div (T_J + 273\ °C)$
Solving the equations above for K gives: $K = P_D \times (T_A + 273\ °C) + \theta_{JA} \times (PD)^2$
where K is a constant pertaining to the particular part. K can be determined by measuring P_D (at equilibrium) for an known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving the above equations iteratively for any value of T_A.

6 Peripheral operating requirements and behaviors

6.1 Core modules

6.1.1 SWD electricals

Table 13. SWD full voltage range electrical

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	5.5	V
J1	SWD_CLK frequency of operation • Serial wire debug	0	20	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	5	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	5	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	41	ns

6.2 External oscillator (OSC) and ICS characteristics

6.2.1 External oscillator(OSC) characteristics

Table 14. OSC specifications (temperature range = -40 to 125 °C ambient)

Num	C	Characteristic	Symbol	Min	Typical	Max	Unit
1	C	Crystal frequency	f_{hi}	4	—	30	MHz
2	D	Load capacitors	CL1, CL2	See Note1			
3	D	Series resistor	R_S	—	0	—	kΩ
4	C	Crystal start-up time	t_{CST}		3		ms

Note 1: For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors designed for high-frequency applications, and selected to match the requirements of the crystal. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

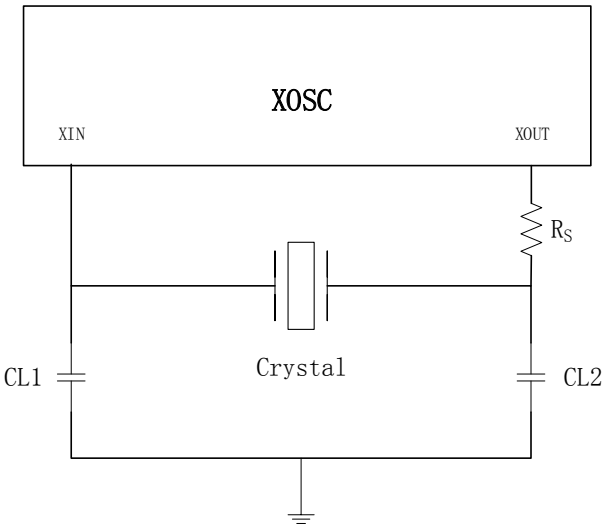

Figure 4. Typical crystal or resonator circuit

6.2.2 Internal RC characteristics

Table 15. OSC and ICS specifications (temperature range = -40 to 125 °C ambient)

Num	C	Characteristic		Symbol	Min	Typical	Max	Unit
1	P	LFOSC output frequency range	Over temperature range from -40 °C to 125°C	f_{lfosc}	7.90	8	8.10	MHz
2	C	LFOSC Deviation of IRC over temperature when trimmed at T = 25 °C, VDD = 2.7-5.5 V	Over temperature range from -40 °C to 125°C	Δfint_t	-1.1		1.1	%
3	P	LPOSC Internal reference clock frequency,factory trimmed,	T = 25 °C, VDD = 5 V	fint_ft	—	32	—	kHz
4	P	LPOSC Factory trimmed internal oscillator accuracy	T = 25 °C, VDD = 5 V	Δfint_ft	-1.5	—	1.5	%
5	C	LPOSC Deviation of IRC over temperature when trimmed at T = 25 °C, VDD = 2.7-5.5 V	Over temperature range from -40 °C to 125°C	Δfint_t	-10	—	+10	%

6.2.3 PLL characteristics

Table 16. PLL characteristics

No.	Symbol	Parameter	Min	Typ	Max	Unit
1	fPLL_IN	PLL input clock frequency	4		30	MHz

No.	Symbol	Parameter	Min	Typ	Max	Unit
2	fPLL_REF	PFD input clock frequency			8	MHz
3	fPLL_OUT	PLL output clock frequency	125		1500	MHz
4	fVCO_OUT	VCO output frequency	500		1500	MHz
Operatng condition: junction temperature -40~125°C fPLL_OUT is fVCO_OUT /Postdiv, Postdiv can be 1,2 4; fPLL_REF is fPLL_IN_ /Prediv, Prediv can be 1,2,4.						

6.3 Embedded flash specifications

This section provides details about program/erase times and program/erase endurance for the flash memories.

Table 17. Flash characteristics

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage for program/erase - 40°C to 125 °C	$V_{prog/erase}$	2.7	—	5.5	V
D	Supply voltage for read operation	V_{Read}	2.7	—	5.5	V
D	Flash Bus frequency	f_{SYS}	8	96	100	MHz
D	Read Once	t_{RDONCE}	1	2	2	t_{cyc}
D	Mass Erase (all Main Block pages)	t_{MER}	—	114.6	—	ms
D	Page Erase (one page)	t_{PER}	—	114.6	—	ms
D	Mass Erase Verify	t_{MERV}	65600	—	131200	t_{cyc}
D	Page Erase Verify	t_{PERV}	535	—	1070	t_{cyc}
D	Program Flash (1 word)	t_{PRG1}		66.5		us
D	Program Flash (n word, n>1)	t_{PRGn}		66.5+14.6× (n-1)		us
C	FLASH Program/erase endurance T_A = -40 °C to 125 °C	n_{EDR}	10 k	—	—	Cycles
C	Data retention at an average junction temperature of T_{Javg} = 85°C after up to 10,000 program/erase cycles	t_{RET}	10	—	—	years

Note: t_{cyc} = 1/ f_{SYS}.

6.4 Analog

6.4.1 ADC characteristics

Table 18. 12 bit ADC Operating Conditions and Characteristics

Symbol	Parameter	Condition	MIN.	TYP.	MAX.	UNIT
V_{AVDD}	Supply Voltage	Absolute	2.7	-	5.5	V
V_{IN}	Input Voltage Range	-	0	-	V_{AVDD}	V

Symbol	Parameter	Condition	MIN.	TYP.	MAX.	UNIT
R_{IN}	Internal input impedance	-	-	-	5	kΩ
V_{REF}	Buffer Output	-	1.35	-	2.75	V
C_{ADC}	Internal Sampling Capacitor	-	-	2.3	-	pF
R_{ADC}	Sampling switch resistance	-	-	2.6	-	kΩ
f_{ADC}	ADC clock frquency	-	-	-	10	MHz
f_{sample}	Sampling Time	-	350	-	-	ns
f_{trig}	Trigger Frequency	f_{ADC}=10MHz	-	-	500	kHz
INL	Integral Non-Linearity	-	-	1.5	-	LSB
DNL	Differential Non-Linearity	-	-	1.5	-	LSB
CH	External Channels	-	-	-	16	-

Table 19. 12 bit ADC Operating Conditions and Characteristics(continue)

Characteristic	Conditions	C	Symbol	Min	Typ1	Max	Unit
Temp sensor slope	-40 °C–125 °C	D	m	--	1.629	--	mV/°C
Temp sensor voltage	25 °C	D	VTEMP25	--	0.72[1]	--	V

[1]: 25°C offset store in 0x40003050[18:13], bit18 is sign bit, [17:13] every bit is 0.5°C offset with 25°C

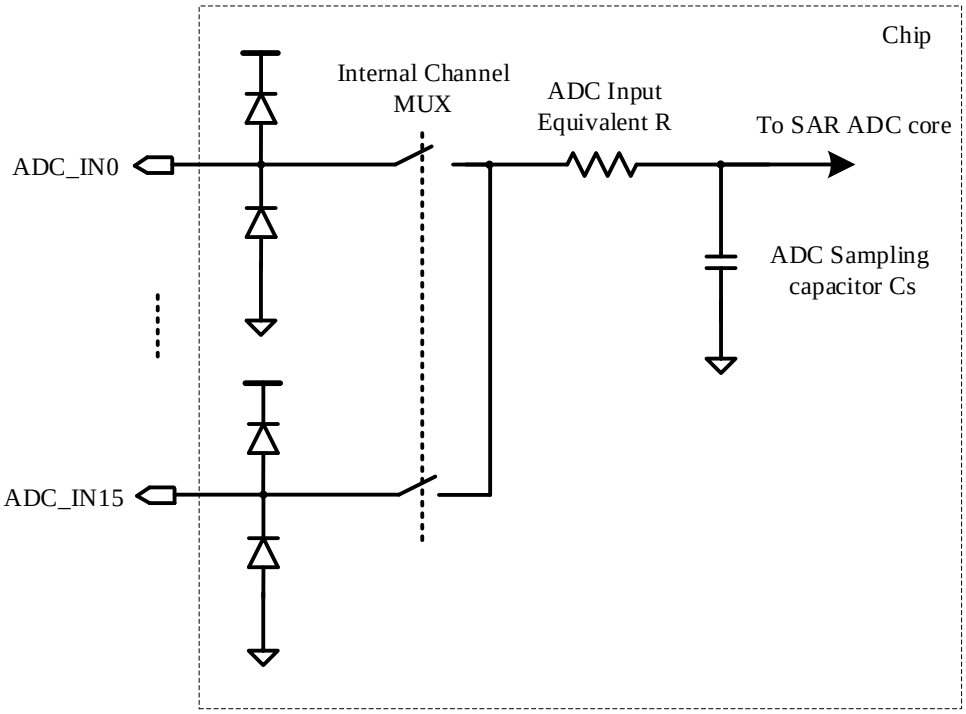

Figure 5. ADC input equivalent diagram

6.4.2 Analog comparator (ACMP) electricals

Table 20. Comparator electrical specifications

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	V_{AVDD}	2.5	—	5.5	V
T	Supply current (Operation mode)	I_{DDA}	—		20	μA
D	Analog input voltage	V_{AIN}	V_{SS} - 0.3	—	V_{AVDD}	V
P	Analog input offset voltage	V_{AIO}	—	—	40	mV
C	Analog comparator hysteresis (HYST=0)	V_H	—	20	—	mV
C	Analog comparator hysteresis (HYST=1)	V_H	—	30	—	mV
T	Supply current (Off mode)	I_{DDAOFF}	—		100	nA
C	Propagation Delay	t_D	—	0.4	1	μs

6.5 Communication interfaces

6.5.1 SPI switching specifications

The serial peripheral interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's reference manual for information about the modified transfer formats used for communicating with slower peripheral devices. All timing is shown

with respect to 20% VDD and 80% VDD, unless noted, and 25 pF load on all SPI pins. All timing assumes slew rate control is disabled and high-drive strength is enabled for SPI output pins.

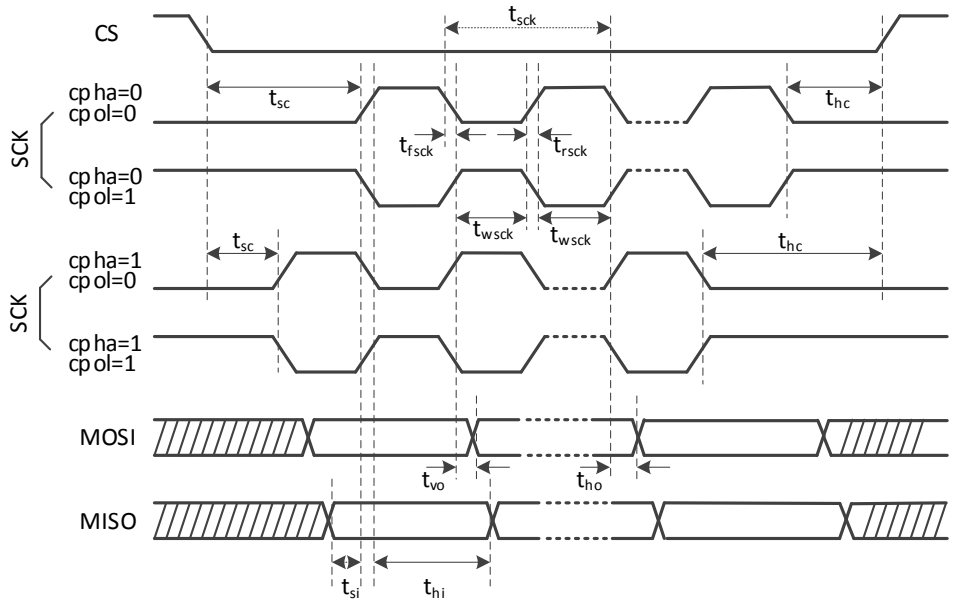

Figure 6. SPI timing diagram – master

Table 21. SPI characteristics – master

Symbol	Description	Min.	Max.	Unit	Comment
f_{op}	Frequency of operation	f_{bus}/512	f_{bus}/2	Hz	f_{bus} is bus clock
t_{sc}	CS setup time	1×t_{bus}	256×t_{bus}	ns	Negative edge of CS to first SCK edge
t_{hc}	CS hold time	1×t_{bus}	256×t_{bus}	ns	Last SCK edge to positive edge of CS
t_{wsck}	SCK high or low level time	1×t_{bus}	256×t_{bus}	ns	No considering **t_{rsck}** and **t_{fsck}**
t_{si}	Data input setup time	8	-	ns	
t_{hi}	Data input hold time	8	-	ns	
t_{vo}	Data output valid time	-	25	ns	
t_{ho}	Data output hold time	1	-	ns	
t_{rsck}	Clock output rise time				
t_{fsck}	Clock output fall time				

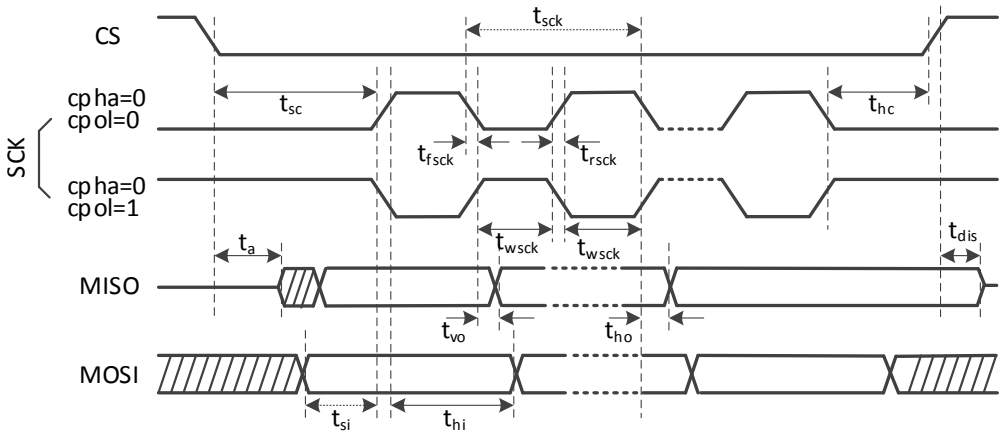

Figure 7. SPI timing diagram – slave(cpha=0)

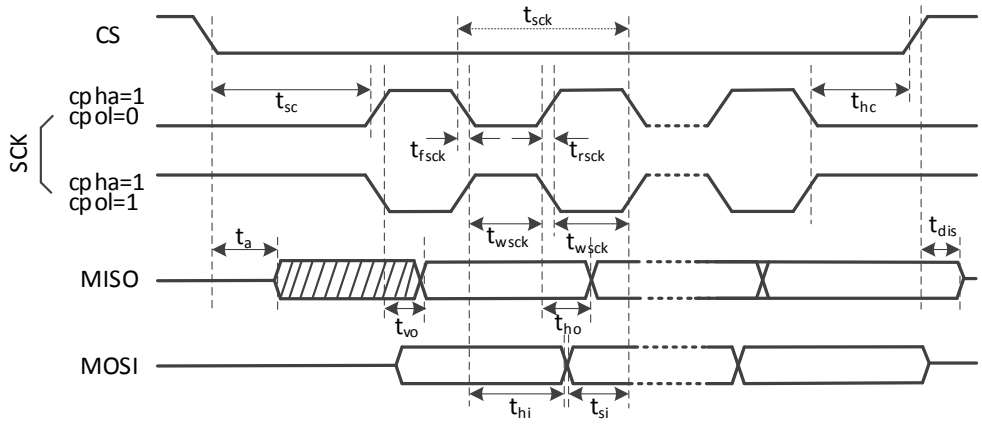

Figure 8. SPI timing diagram – slave(cpha=1)

Table 22. SPI characteristics - slave

Symbol	Description	Min.	Max.	Unit	Comment
f_{op}	Frequency of operation	-	18M	Hz	
t_{sc}	CS setup time	2×t_{bus}	-	ns	Negative edge of CS to first SCK edge
t_{hc}	CS hold time	2×t_{bus}	-	ns	Last SCK edge to positive edge of CS
t_a	slave access time	-	t_{bus}	ns	Data from “Z” to effective
t_{dis}	slave MISO disable time	-	t_{bus}	ns	Data from effective to “Z”
t_{wsck}	SCK high or low level time	30%	70%		
t_{si}	Data input setup time	12	-	ns	
t_{hi}	Data input hold time	12	-	ns	
t_{vo}	Data output valid time	-	35[1] 29[2]	ns	
t_{ho}	Data output hold time	12	-	ns	
t_{rsck}	Clock input rise time				
t_{fsck}	Clock input fall time				

[1]: GPIO setting 00
[2]: GPIO setting 10

6.5.2 CAN

Table 23. CAN wake-up pulse characteristics

Parameter	Symbol	Min	Typ	Max	Unit
CAN wakeup dominant pulse filtered	t_{WUP}	-	-	0.9	µs
CAN wakeup dominant pulse pass	t_{WUP}	4.7	-	-	µs

7 Dimensions

7.1 LQFP64 package information

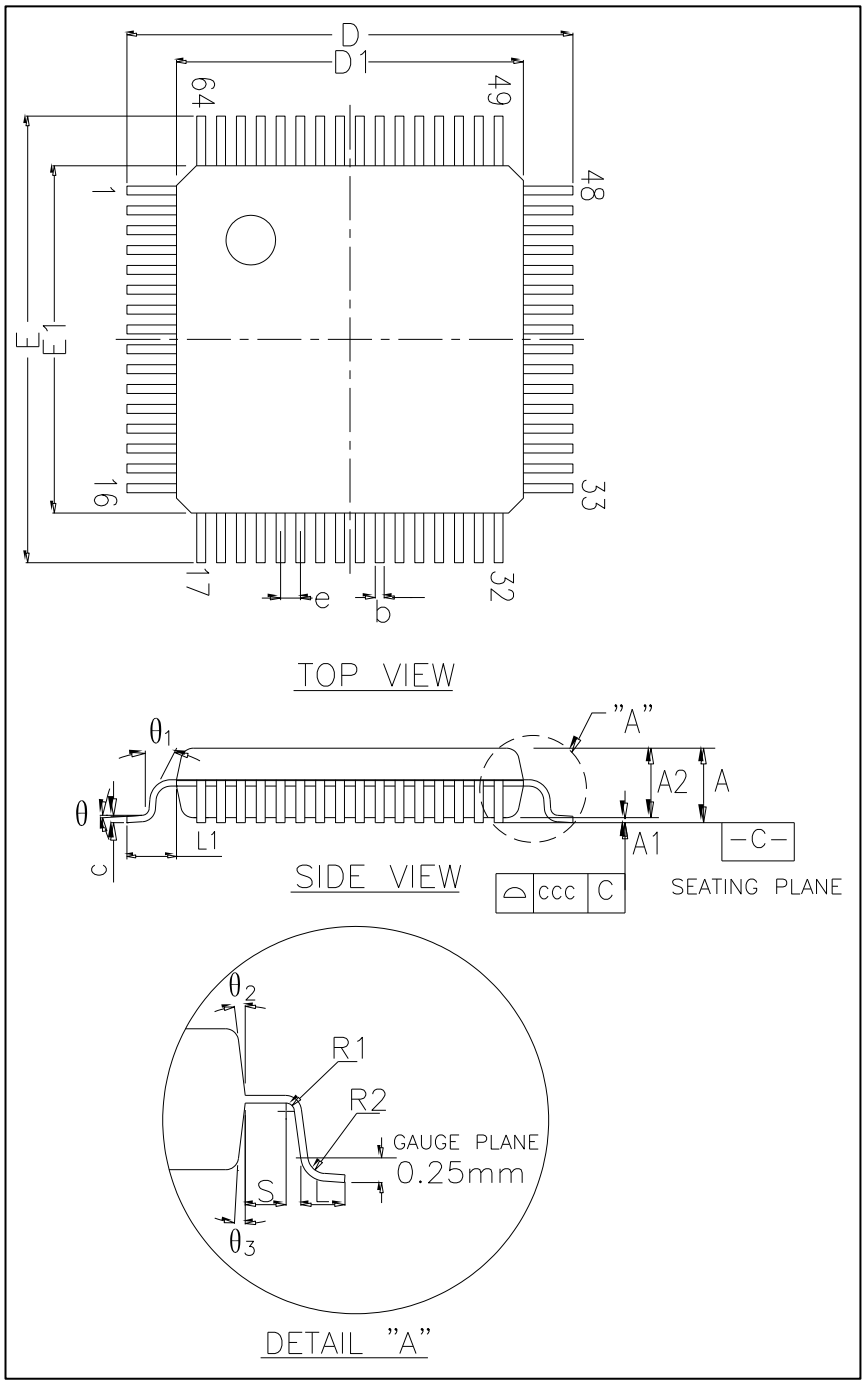

Figure 9. LQFP64 - 64-pin, 7 x 7 mm low-profile quad flat package outline

1. Drawing is not to scale.

Table 24. LQFP64 - 64-pin, 7 x 7 mm low-profile quad flat package mechanical data

ITEM		SYMBOL	MIN.	NOM.	MAX.
Total height		A	—	—	1.60
Stand off		A1	0.05	—	0.15
Mold thickness		A2	1.35	1.40	1.45
Lead width		b	0.13	0.18	0.23
Outer Lead Distance	X	D	9.00 BSC.		
	Y	E	9.00 BSC.		
Package size	X	D1	7.00 BSC.		
	Y	E1	7.00 BSC.		
Lead pitch		e	0.40 BSC.		
R2		R2	0.08	—	0.20
R1		R1	0.08	—	—
Angle		Θ	0°	3.5°	7°
Angle 1		Θ1	0°	—	—
Angle 2		Θ2	11°	12°	13°
Angle 3		Θ3	11°	12°	13°
L/F thickness		c	0.09	—	0.20
L		L	0.45	0.60	0.75
Lead length		L1	1.00 REF		
S		S	0.20	—	—
Lead profile of a surface		ccc	0.08		

1. Dimensions are expressed in millimeters.

Device Marking for LQFP64

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

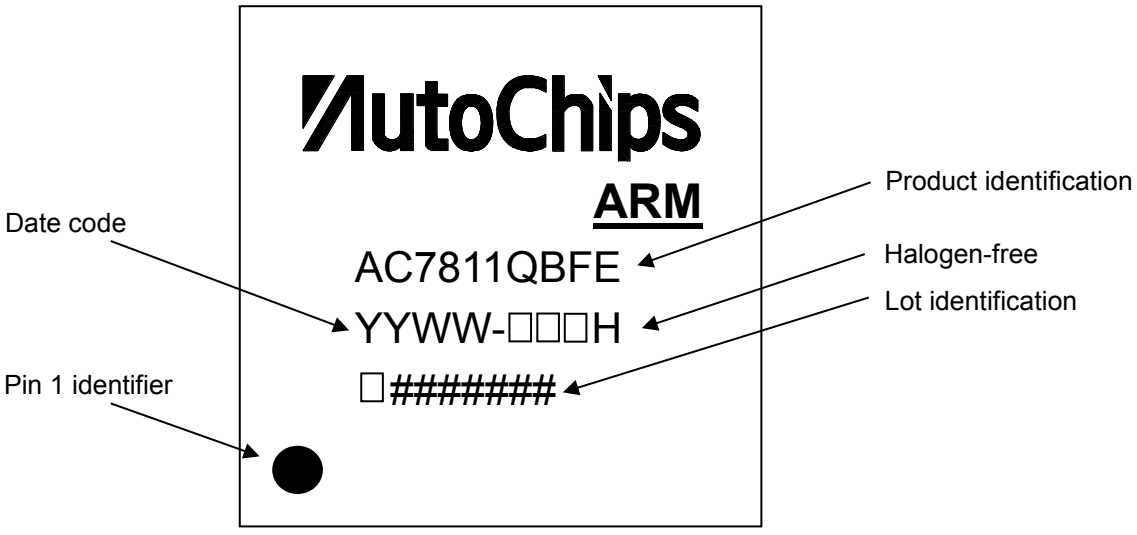

Figure 10. LQFP64 marking example (package top view)

7.2 LQFP80 package information

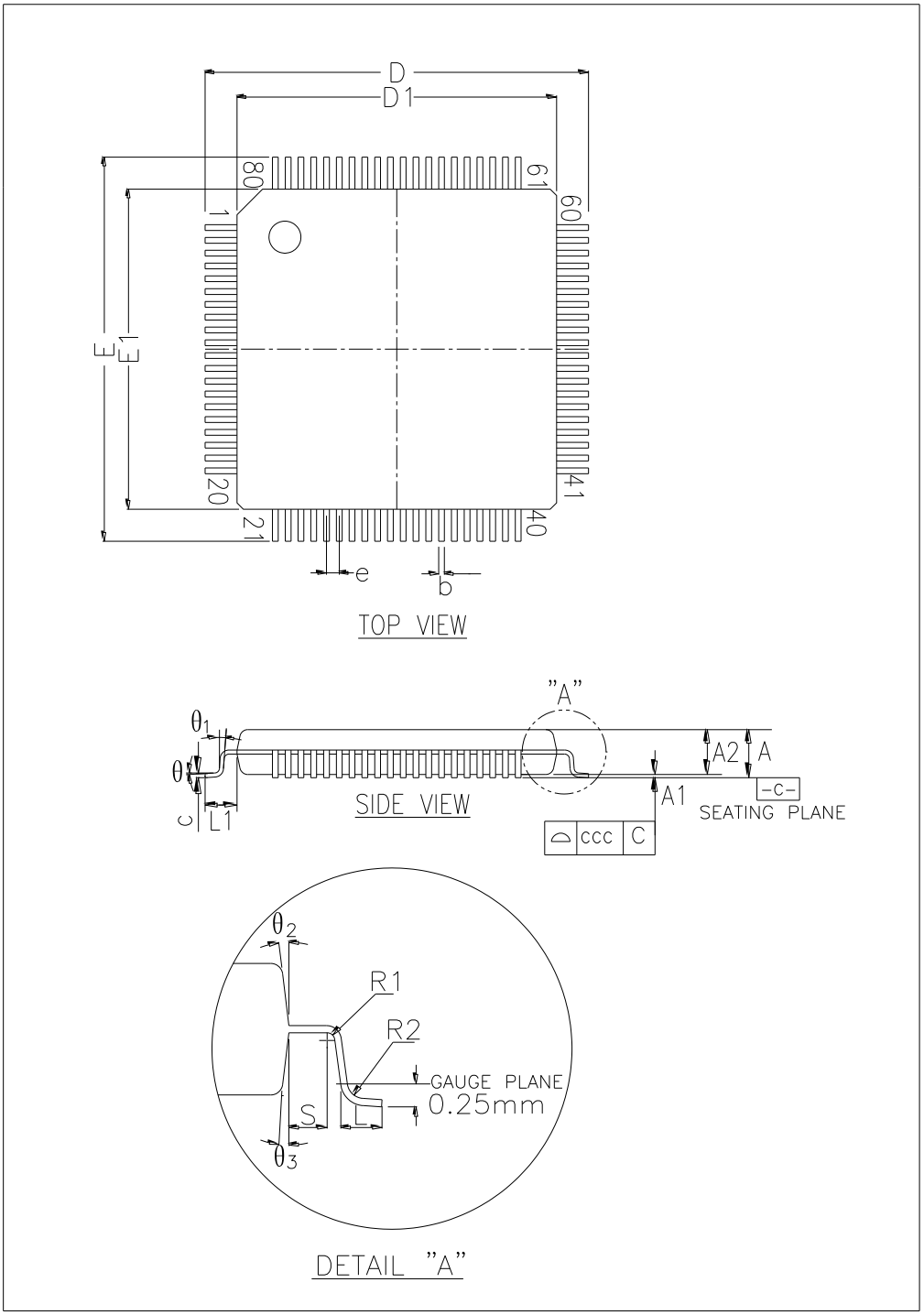

Figure 11. LQFP80 - 80-pin, 10 x 10 mm low-profile quad flat package outline

1. Drawing is not to scale.

Table25. LQFP80 - 80-pin, 10 x 10 mm low-profile quad flat package mechanical data

ITEM		SYMBOL	MIN.	NOM.	MAX.
Total height		A	—	—	1.60
Stand off		A1	0.05	—	0.15
Mold thickness		A2	1.35	1.40	1.45
Lead width		b	0.13	0.18	0.23
Outer Lead Distance	X	D	12.00 BSC.		
	Y	E	12.00 BSC.		
Package size	X	D1	10.00 BSC.		
	Y	E1	10.00 BSC.		
Lead pitch		e	0.40 BSC.		
R2		R2	0.08	—	0.20
R1		R1	0.08	—	—
Angle		Θ	0°	3.5°	7°
Angle 1		Θ1	0°	—	—
Angle 2		Θ2	11°	12°	13°
Angle 3		Θ3	11°	12°	13°
L/F thickness		c	0.09	—	0.20
L		L	0.45	0.60	0.75
Lead length		L1	1.00 REF		
S		S	0.20	—	—
Lead profile of a surface		ccc	0.08		

1. Dimensions are expressed in millimeters.

Device Marking for LQFP80

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

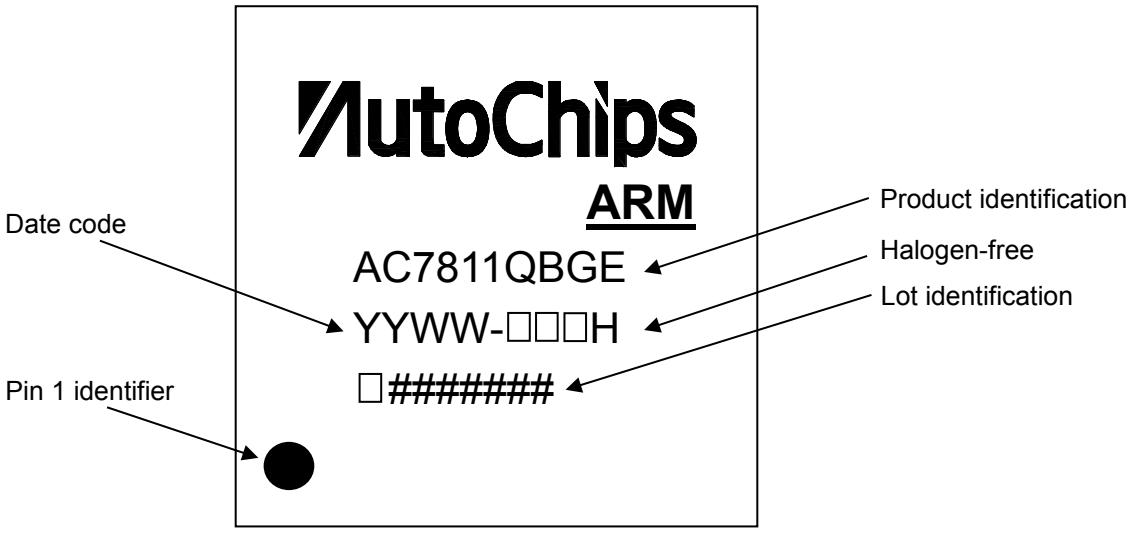

Figure 12. LQFP80 marking example (package top view)

8 Pinout

8.1 Signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

Table26. Signal multiplexing and pin assignments

80 LQFP	64 LQFP	PIN Name	function 0	function 1	function 2	function 3	PINMUX	GPIO (NUM)
1	1	PA0	PA0	SPI1_NSS	TRACED3	FLASH_NSS	PMUX0[2:0]	0
2	2	PA1	PA1	SPI1_SCK	TRACECLK	FLASH_SCK	PMUX0[5:3]	1
3	3	PA2	PA2	SPI1_MISO	TRACED0	FLASH_DQ1	PMUX0[8:6]	2
4	4	PA3	PA3	SPI1_MOSI	TRACED1	FLASH_DQ0	PMUX0[11:9]	3
5	5	PA4	PA4	UART4_TX	CAN1_RX	FLASH_DQ3	PMUX0[14:12]	4
6	6	PA5	PA5	UART4_RX	CAN1_TX	FLASH_DQ2	PMUX0[17:15]	5
7		PD3	PD3	PWM1_CH0	HWLIN_TX		PMUX5[5:3]	51
8		PD4	PD4	PWM1_CH1	HWLIN_RX		PMUX5[8:6]	52
9		PD5	PD5	PWM_EXT	CAN1_STDBY		PMUX5[11:9]	53
10	7	OSC_OUT	OSC_OUT[1]					
11	8	OSC_IN	OSC_IN[1]					
12	9	AVSS	AVSS					
13	10	AVDD	AVDD					
14	11	AVDD	AVDD					
15	12	AVSS	AVSS					
16	13	PA6	PA6	ADC_IN10	UART1_CTS	UART4_TX	PMUX0[20:18]	6
17		PD6	PD6	ADC_IN12	UART1_RTS	UART4_RX	PMUX5[14:12]	54
18	14	PA7	PA7	ADC_IN0	UART1_TX	UART5_TX	PMUX0[23:21]	7
19	15	PA8	PA8	ADC_IN1	UART1_RX	UART5_RX	PMUX0[26:24]	8
20	16	PA9	PA9	ADC_IN2	SPI2_NSS	HWLIN_TX	PMUX0[29:27]	9
21	17	PA10	PA10	ADC_IN3	SPI2_SCK	HWLIN_RX	PMUX1[2:0]	10
22	18	PA11	PA11	ADC_IN4	SPI2_MISO	UART3_RX	PMUX1[5:3]	11
23	19	PA12	PA12	ADC_IN5	SPI2_MOSI	UART3_TX	PMUX1[8:6]	12
24	20	PA13	PA13	ADC_IN6	I2C1_SCL	UART6_RX	PMUX1[11:9]	13
25	21	PA14	PA14	ADC_IN7	I2C1_SDA	UART6_TX	PMUX1[14:12]	14
26	22	PA15	PA15	ADC_IN8	UART2_RTS		PMUX1[17:15]	15
27	23	PB0	PB0	ADC_IN9	UART2_TX	CAN2_STDBY	PMUX1[20:18]	16

28	24	PB1	PB1	ADC_IN11	UART2_RX		PMUX1[23:21]	17
29		PD7	PD7	ADC_IN13	PWDT_EXT	PWM3_CH0	PMUX5[17:15]	55
30		PD8	PD8	ADC_IN14	CAN2_TX	PWM3_CH1	PMUX5[20:18]	56
31		PD9	PD9	ADC_IN15	CAN2_RX	PWDT_IN0	PMUX5[23:21]	57
32	25	PB2	PB2	NMI_B	UART3_TX	CAN1_STDBY	PMUX1[26:24]	18
33	26	NRST	NRST[1]					
34	27	PB3	PB3	PWDT_IN1	UART3_RX		PMUX1[29:27]	19
35	28	PB4	PB4	PWDT_IN2	TRACED2		PMUX2[2:0]	20
36	29	PB5	PB5	UART1_TX	PWDT_IN1		PMUX2[5:3]	21
37	30	PB6	PB6	UART1_RX	PWDT_IN2	PWM3_CH0	PMUX2[8:6]	22
38	31	PB7	PB7	UART1_RTS	PWM_FAULT1		PMUX2[11:9]	23
39		PD10	PD10	PWM_FAULT1	I2C2_SCL		PMUX5[26:24]	58
40	32	PB8	PB8	PWDT_IN0	I2C2_SDA		PMUX2[14:12]	24
41	33	PB9	PB9	PWM0_CH0	PWM2_CH0	CAN1_RX	PMUX2[17:15]	25
42	34	DVSS	DVSS					
43	35	DVDD	DVDD					
44	36	VPP	VPP					
45	37	PB10	PB10	PWM0_CH1	PWM2_CH1	CAN1_TX	PMUX2[20:18]	26
46	38	PB11	PB11	SPI2_NSS	PWM2_CH2		PMUX2[23:21]	27
47	39	PB12	PB12	SPI2_SCK	PWM2_CH3		PMUX2[26:24]	28
48	40	PB13	PB13	SPI2_MISO	PWM2_CH4	UART5_TX	PMUX2[29:27]	29
49	41	PB14	PB14	SPI2_MOSI	PWM2_CH5	UART5_RX	PMUX3[2:0]	30
50		PD11	PD11	UART5_TX	UART3_RTS		PMUX5[29:27]	59
51		PD12	PD12	UART5_RX	UART4_RTS		PMUX6[2:0]	60
52		PD13	PD13	PWM2_CH4	UART5_RTS		PMUX6[5:3]	61
53		PD14	PD14	PWM2_CH5	UART6_RTS		PMUX6[8:6]	62
54	42	PB15	PB15	PWM2_CH0	PWM0_EXT		PMUX3[5:3]	31
55	43	PC0	PC0	PWM2_CH1	PWM1_EXT		PMUX3[8:6]	32
56	44	PC1	PC1	PWM2_CH2	UART5_RTS		PMUX3[11:9]	33
57	45	PC2	PC2	PWM2_CH3	UART6_RTS		PMUX3[14:12]	34
58	46	PC3	PC3	UARTTX_ SFLASH[1]	PWM2_CH4	PWM2_CH0	PMUX3[17:15]	35
59	47	PC4	PC4	UARTRX_ SFLASH[1]	PWM2_CH5	PWM2_CH1	PMUX3[20:18]	36
60	48	PC5	PC5	I2C2_SCL	UART1_CTS		PMUX3[23:21]	37
61	49	PC6	PC6	I2C2_SDA	UART1_CTS		PMUX3[26:24]	38
62	50	PC7	PC7	JTCK_SWCLK[1]	UART3_RTS		PMUX3[29:27]	39
63	51	PC8	PC8	JTDO_ TRACESWO[1]	UART2_RTS		PMUX4[2:0]	40
64	52	PC9	PC9	JTMS_SWDIO[1]	UART4_RTS	PWM_FAULT1	PMUX4[5:3]	41

65	53	PC10	PC10	CAN2_TX	UART6_TX	PWM_FAULT2	PMUX4[8:6]	42
66	54	PC11	PC11	CAN2_RX	UART6_RX	PWDT_IN0	PMUX4[11:9]	43
67		PD15	PD15	JTDI[1]	CAN1_STDBY	PWDT_IN1	PMUX6[11:9]	63
68	55	BOOT	PE3	BOOT[1]				
69	56	PC12	PC12	I2C1_SCL	UART5_TX		PMUX4[14:12]	44
70	57	PC13	PC13	I2C1_SDA	UART5_RX		PMUX4[17:15]	45
71	58	DVSS	DVSS					
72	59	DVDD	DVDD					
73		PE0	PE0	NJTRST[1]	CAN2_STDBY	PWDT_IN2	PMUX6[14:12]	64
74	60	PC14	PC14	CAN1_RX	UART4_RX	PWDT_IN3	PMUX4[20:18]	46
75	61	PC15	PC15	CAN1_TX	UART4_TX		PMUX4[23:21]	47
76		PE1	PE1	HWLIN_TX	PWM1_CH0		PMUX6[17:15]	65
77		PE2	PE2	HWLIN_RX	PWM1_CH1		PMUX6[20:18]	66
78	62	PD0	PD0	UART1_CTS	PWM_FAULT2		PMUX4[26:24]	48
79	63	PD1	PD1	UART2_TX	PWM0_CH0	I2C2_SCL	PMUX4[29:27]	49
80	64	PD2	PD2	UART2_RX	PWM0_CH1	I2C2_SDA	PMUX5[2:0]	50

Note:

1、 This functions as default function.

2、 All the pins are default as gpio on the first time power on except some dedicated pins.

Eg: if we want to configure PIN1 as SPI1_NSS, we should set PMUX0[2:0]=1.

8.2 Device pin assignment

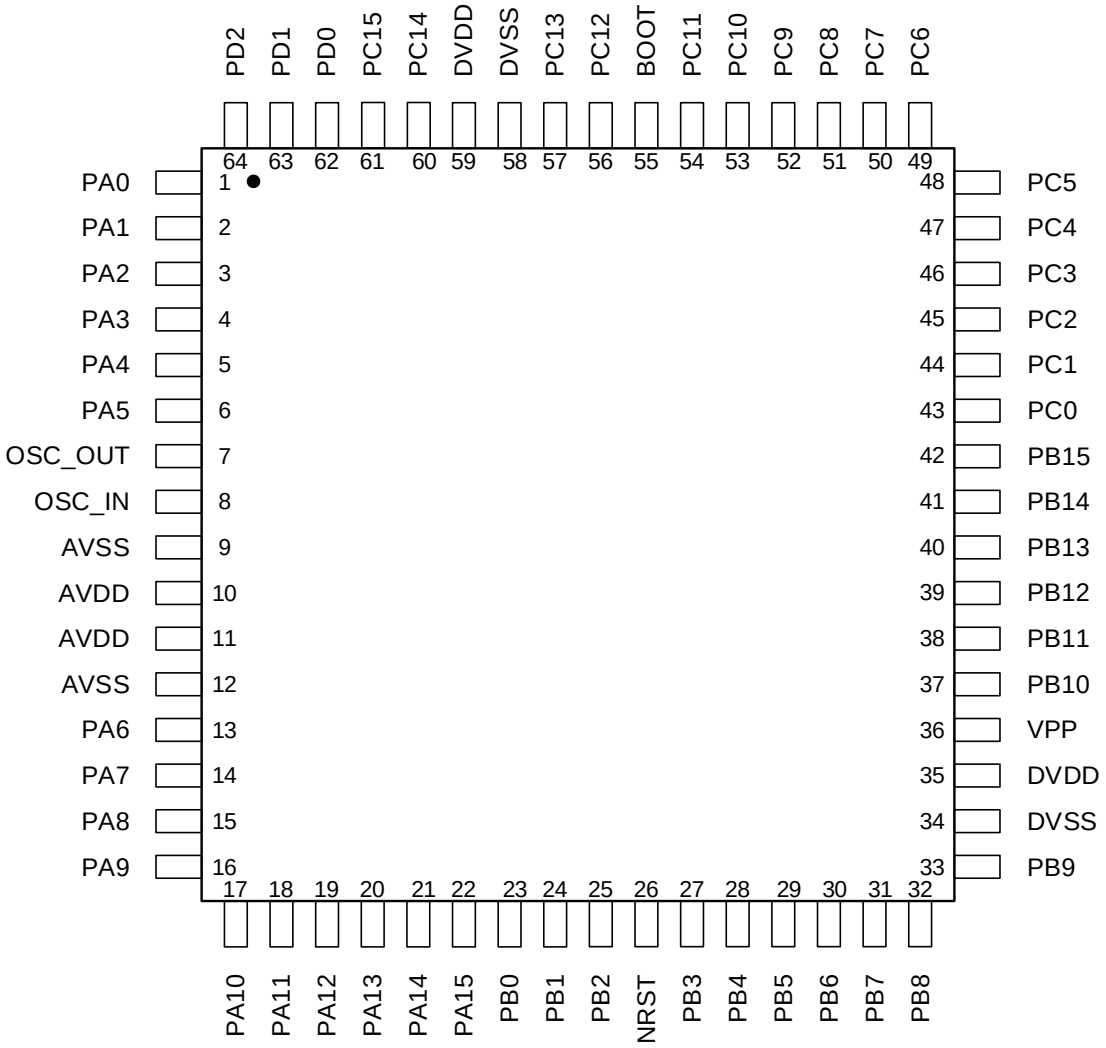

Figure 13. 64-pin LQFP package

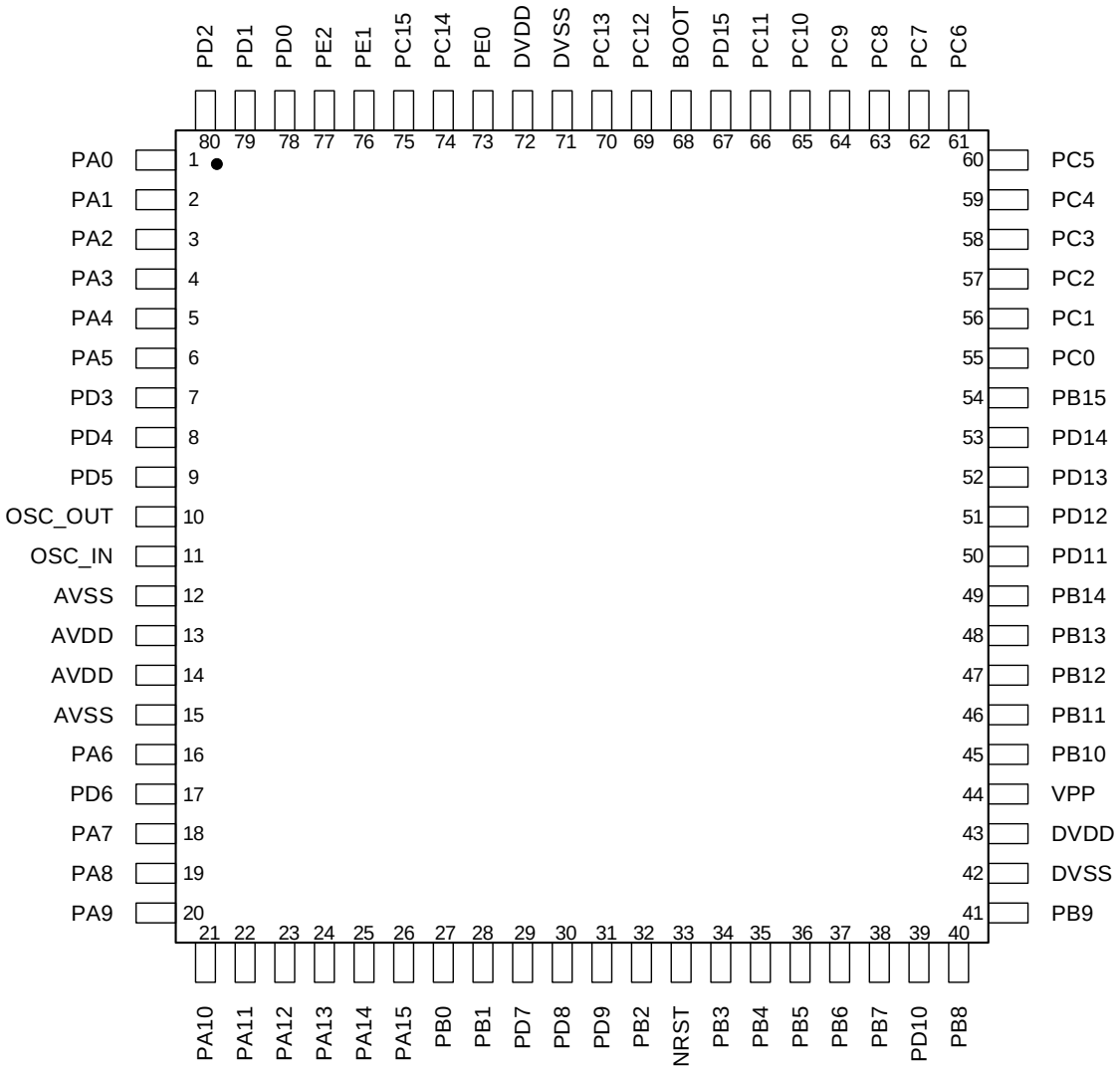

Figure 14. 80-pin LQFP package