AC7802x Data Sheet

Supports the following:

AC78022MBQA， AC78022PBTA

Version: 0.1

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Document Revision History

Revision	Date	Author	Description
0.1	2022-10-15	AutoChips	Initial draft

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1 Key features

- **Automotive grade**
  - AEC-Q100 Grade 1 qualified
- **Performance**
  - Up to 32 MHz ARM® Cortex-M0+ core
  - Single cycle 32-bit multiplier
  - Fast I/O access port
- **Memories and memory interfaces**
  - 32 KB Flash
  - 2KB Dflash
  - 4 KB SRAM, ECC is supported
- **Clocks**
  - Oscillator (OSC) - supports 8 MHz to 20 MHz crystal or ceramic resonator; choice of low power or high gain oscillators
  - Internal clock source (RC) - internal RC, 32 MHz internal clock source can be generated
  - Internal 32 kHz low-power oscillator (LPO)
- **System peripherals**
  - Power management module (PMC) with two power modes: Run, Stop
  - Low-voltage detection (LVD) with reset
  - Watchdog with independent clock source(WDG)
  - Serial wire debug (SWD) interfaces
- **Human-machine interface**
  - Up to 27 general-purpose input/output (GPIO)
  - External interrupt (IRQ)
- **Analog modules**
  - One up to 18-channel 12-bit 250Ksps SAR ADC, optional hardware trigger (ADC)
  - One analog comparators containing a 6-bit DAC and programmable reference input(ACMP)
- **Timers**
  - Two 2-chaneel and one 4-channel PWM
  - Four 32-bit periodic interrupt timer (TIMER)
  - One pulse width timer (PWDT)
  - One real-time clock (RTC)
- **Communication interfaces**
  - Two UART modules (one support Software LIN)
  - One SPI modules (SPI)
  - One I2C modules (I2C)

- **Operating characteristics**
  - Voltage range: 2.7 to 5.5 V
  - Temperature range (ambient): -40 to 125°C
- **Package options**
  - 32-pin HVQFN
  - 20-pin TSSOP

2 Block diagram

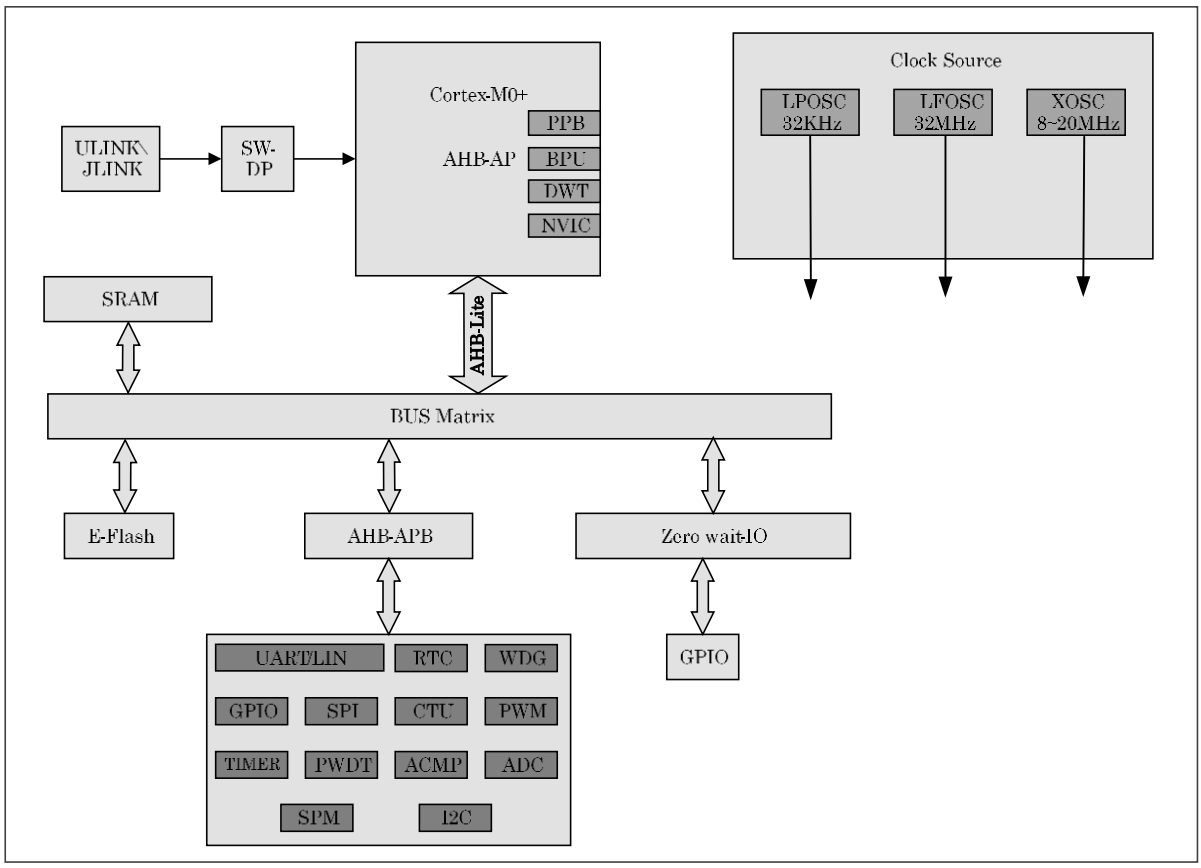


Figure 2-1 AC7802x Block Diagram

3 Part identification

3.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

3.2 Format

Part numbers for this device have the following format:

AC## GTUFPN

3.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Table 3-1 Fields

Field	Description	Values
AC	Autochips	• AC
7	AutoChips MCU family	• 7
8	General Purpose Automotive MCU	• 8
0	Core Platform	• 0= Cortex-M0+
2	Specific Function Bit	• 1 = performance/version bit • 2 = Product subfamily 2: CAN-FD/CAN is not supported
2		
M	Pin Count	• P = 20 • M = 32
B	Flash Memory Size	• B = 32 KB
Q	Package type	• Q = QFN • T = TSSOP
A	Temperature range(°C)	• A= AEC-Q100 Grade 1(-40~125°C) • I= -40~105°C • C= -40~85°C
/x	Internal identification, only the packaging P/N suffix is used	/A or /B and so on

3.4 Example

This is an example part number: AC78022MBQA.

4 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate.

Table 4-1 Parameter classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

5 Ratings

5.1 Thermal handling ratings

Table 5-1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, High Temperature Storage Life.
2. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

5.2 Moisture handling ratings

Table 5-2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

5.3 ESD handling ratings

Table 5-3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	–4000	4000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	–750	750	V	2
I_{LAT}	Latch-up current at ambient temperature of 125°C	–100	100	mA	3

1. Determined according to AEC-Q100-002-D, HUMAN BODY MODEL ELECTROSTATIC DISCHARGE TEST.
2. Determined according to AEC-Q100-011-C1, CHARGED DEVICE MODEL (CDM) ELECTROSTATIC DISCHARGE TEST.
3. Determined according to AEC-Q100-004-D, IC LATCH-UP TEST.
   - Test was performed at 125 °C case temperature (Class II).
   - Supply groups pass 1.5 V_{ccmax}.

5.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in the following table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this document.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pullup resistor associated with the pin is enabled.

Table 5-4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	6	V
I_{DD}	Maximum current into VDD	—	60	mA
V_{IN}	Input voltage except true open drain pins	–0.3	V_{DD} + 0.3 [1]	V
	Input voltage of true open drain pins	–0.3	V_{DD} + 0.3 [1]	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–20	20	mA

[1] Maximum rating of V_{DD} also applies to V_{IN}.

6 General

6.1 Nonswitching electrical specifications

6.1.1 Power and ground pins

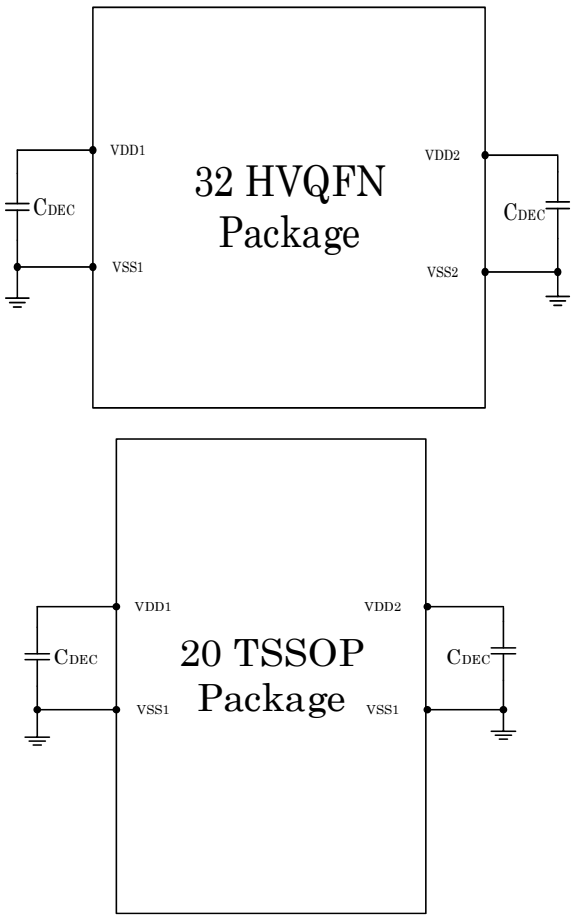


Figure 6-1 Pinout decoupling

1. V_{DD1} and V_{DD2} must be shorted to a common source on PCB.
2. All decoupling capacitors must be low ESR ceramic capacitors(X7R type), the recommended value is 0.1 uF.
3. For improved performance, it is recommended to use 10 uF, 0.1 uF and 1 nF capacitors in parallel.
4. All decoupling capacitors should be placed as close as possible to the corresponding power and ground pins.

6.1.2 DC characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 6-1 DC characteristics

Symbol	C	Descriptions			Min.	Typ.	Max.	Unit
—	—	Operating voltage		—	2.7	—	5.5	V
V_{OH}	P	Output high voltage	drive strength	5 V, I_{load} = -5, -10, -15, -20mA	0.8×V_{DD}	—	—	V
	C			3 V, I_{load} = –3.6, -7.2,-10.8,-14.4 mA	0.8×V_{DD}	—	—	V
I_{OHT}	D	Output high current	Max total I_{OH} for all ports	5 V	—	—	30	mA
				3 V	—	—	20	
V_{OL}	P	Output low voltage	drive strength	5 V, I_{load} = 5, 10, 15, 20mA	—	—	0.8	V
	C			3 V, I_{load} = 3.6, 7.2,10.8,14.4 mA	—	—	0.8	V
I_{OLT}	D	Output low current	Max total I_{OL} for all ports	5 V	—	—	30	mA
				3 V	—	—	20	
V_{IH}	P	Input high voltage	All digital inputs	4.5≤V_{DD}<5.5 V	0.65×V_{DD}	—	V_{DD} + 0.3	V
				2.7≤V_{DD}<4.5 V	0.70×V_{DD}	—	V_{DD} + 0.3	
V_{IL}	P	Input low voltage	All digital inputs	4.5≤V_{DD}<5.5 V	-0.3	—	0.35×V_{DD}	V
				2.7≤V_{DD}<4.5 V	-0.3	—	0.30×V_{DD}	
V_{hys}	C	Input hysteresis	All digital inputs	—	0.06×V_{DD}	—	—	mV
I_{In}	P	Input leakage current	Per pin (pins in high impedance input mode)	V_{IN} = V_{DD} or V_{SS}	-1	0.1	1	μA
R_{PU}	P	Pullup resistors	All digital inputs, when enabled	—	40	75	190	KΩ

R_{PD}	P	Pulldown resistors	All digital inputs, when enabled	—	40	75	190	KΩ
I_{IC}	D	DC injection current	Single pin limit	$V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$	-2	—	2	mA
			Total MCU limit, includes sum of all stressed pins		-5	—	25	
C_{In}	C	Input capacitance, all pins		—	—	5	7	pF
V_{RAM}	C	RAM retention voltage		—	2	—	—	V

Table 6-2 LVD /POR / AVDD Voltage warning specification

Symbol	C	Description	Min.	Typ.	Max.	Unit
V_{POR}	D	POR re-arm voltage [1]	1.6	1.8	2	V
V_{LVRL}	C	Falling low-voltage detect threshold—low range (LVDV= 0)	2.5	2.6	2.7	V
V_{LVRH}	C	Falling low-voltage detect threshold—high range (LVDV=1) [2]	4.2	4.3	4.4	V
V_{HYSLVR}	C	low-voltage detect hysteresis	—	50	—	mV
V_{LVDL}	C	Falling low-voltage warning threshold—high range	2.8	2.9	3.0	V
V_{LVDH}	C	Falling low-voltage warning threshold—low range	4.5	4.6	4.7	V
V_{HYSLVD}	C	Program low-voltage detect hysteresis	—	50	—	mV
V_{BG}	P	Buffered bandgap output [3]	1.18	1.2	1.22	V

[1] Maximum is the highest voltage that POR is guaranteed.

[2] Hysteresis = rising thresholds - falling threshold.

[3] Voltage Factory trimmed at V_{DD} = 5.0 V, Temp = 25 °C.

6.1.3 Supply current characteristics

Table 6-3 Supply current characteristics

Parameter	Symbol	Core/BusFreq	V_{DD} (V)	-40℃	25℃[1]	85℃	105℃	125℃ [2]	Unit
LFOSC, all modules clocks enabled		32/16 MHz	5	TBD	TBD	TBD	TBD	TBD	mA
		16/16 MHz		TBD	TBD	TBD	TBD	TBD	
		16/8 MHz		TBD	TBD	TBD	TBD	TBD	
		8/8 MHz		TBD	TBD	TBD	TBD	TBD	
		2/2 MHz		TBD	TBD	TBD	TBD	TBD	
		32/16 MHz	3.3	TBD	TBD	TBD	TBD	TBD	
		16/16 MHz		TBD	TBD	TBD	TBD	TBD	
		16/8 MHz		TBD	TBD	TBD	TBD	TBD	
		8/8 MHz		TBD	TBD	TBD	TBD	TBD	
		2/2 MHz		TBD	TBD	TBD	TBD	TBD	
LFOSC,all modules clocks disabled and gated		32/16 MHz	5	TBD	TBD	TBD	TBD	TBD	mA
		16/16 MHz		TBD	TBD	TBD	TBD	TBD	
		16/8 MHz		TBD	TBD	TBD	TBD	TBD	
		8/8 MHz		TBD	TBD	TBD	TBD	TBD	
		2/2 MHz		TBD	TBD	TBD	TBD	TBD	
		32/16 MHz	3.3	TBD	TBD	TBD	TBD	TBD	
		16/16 MHz		TBD	TBD	TBD	TBD	TBD	
		16/8 MHz		TBD	TBD	TBD	TBD	TBD	
		8/8 MHz		TBD	TBD	TBD	TBD	TBD	
		2/2 MHz		TBD	TBD	TBD	TBD	TBD	
XOSC(16M), all modules clocks enabled		16/16 MHz	5	TBD	TBD	TBD	TBD	TBD	mA
		16/8 MHz		TBD	TBD	TBD	TBD	TBD	
		8/8 MHz		TBD	TBD	TBD	TBD	TBD	
		8/4 MHz		TBD	TBD	TBD	TBD	TBD	
		4/4 MHz		TBD	TBD	TBD	TBD	TBD	
		16/16 MHz	3.3	TBD	TBD	TBD	TBD	TBD	
		16/8 MHz		TBD	TBD	TBD	TBD	TBD	
		8/8 MHz		TBD	TBD	TBD	TBD	TBD	
		8/4 MHz		TBD	TBD	TBD	TBD	TBD	
		4/4 MHz		TBD	TBD	TBD	TBD	TBD	
XOSC, all modules clocks disabled and gated		16/16 MHz	5	TBD	TBD	TBD	TBD	TBD	mA
		16/8 MHz		TBD	TBD	TBD	TBD	TBD	
		8/8 MHz		TBD	TBD	TBD	TBD	TBD	
		8/4 MHz		TBD	TBD	TBD	TBD	TBD	
		4/4 MHz		TBD	TBD	TBD	TBD	TBD	

		16/16 MHz	3.3	TBD	TBD	TBD	TBD	TBD	
		16/8 MHz		TBD	TBD	TBD	TBD	TBD	
		8/8 MHz		TBD	TBD	TBD	TBD	TBD	
		8/4 MHz		TBD	TBD	TBD	TBD	TBD	
		4/4 MHz		TBD	TBD	TBD	TBD	TBD	
Sleep mode LFOSC, all modules clocks enabled		32/16 MHz	5	TBD	TBD	TBD	TBD	TBD	mA
		16/16 MHz		TBD	TBD	TBD	TBD	TBD	
		16/8 MHz		TBD	TBD	TBD	TBD	TBD	
		8/8 MHz		TBD	TBD	TBD	TBD	TBD	
		2/2 MHz		TBD	TBD	TBD	TBD	TBD	
		32/16 MHz	3.3	TBD	TBD	TBD	TBD	TBD	
		16/16 MHz		TBD	TBD	TBD	TBD	TBD	
		16/8 MHz		TBD	TBD	TBD	TBD	TBD	
		8/8 MHz		TBD	TBD	TBD	TBD	TBD	
		2/2 MHz		TBD	TBD	TBD	TBD	TBD	
Sleep mode XOSC, all modules clocks enabled		16/16 MHz	5	TBD	TBD	TBD	TBD	TBD	mA
		16/8 MHz		TBD	TBD	TBD	TBD	TBD	
		8/8 MHz		TBD	TBD	TBD	TBD	TBD	
		8/4 MHz		TBD	TBD	TBD	TBD	TBD	
		4/4 MHz		TBD	TBD	TBD	TBD	TBD	
		16/16 MHz	3.3	TBD	TBD	TBD	TBD	TBD	
		16/8 MHz		TBD	TBD	TBD	TBD	TBD	
		8/8 MHz		TBD	TBD	TBD	TBD	TBD	
		8/4 MHz		TBD	TBD	TBD	TBD	TBD	
		4/4 MHz		TBD	TBD	TBD	TBD	TBD	
Stop mode (RTC/GPIO/I2C/SPI/UART/CAN/LIN can wake up) [3]	SI_{DD}	—	5	TBD	TBD	TBD	TBD	TBD	µA
			3.3	TBD	TBD	TBD	TBD	TBD	
ADC enabled adder to Stop mode(mode1)	SI_{DD}	—	5	TBD	TBD	TBD	TBD	TBD	mA
			3.3	TBD	TBD	TBD	TBD	TBD	
ADC(wdt enabled) adder to Stop mode(mode2)	SI_{DD}	—	5	TBD	TBD	TBD	TBD	TBD	
			3.3	TBD	TBD	TBD	TBD	TBD	
ACMP adder to Stop mode	SI_{DD}	—	5	TBD	TBD	TBD	TBD	TBD	
			3.3	TBD	TBD	TBD	TBD	TBD	
				TBD	TBD	TBD	TBD	TBD	
LVD adder to Stop mode	SI_{DD}	—	5	TBD	TBD	TBD	TBD	TBD	µA
			3.3	TBD	TBD	TBD	TBD	TBD	

			3.3	TBD	TBD	TBD	TBD	TBD	

[1] Data in Typical column was characterized at 3.3/5.0 V, 25 °C or is typical recommended value.

[2] Data in Typical column was characterized at 3.3/5.0 V, 125 °C or is typical recommended value.

[3] RTC adder cause <1 μA IDD increase typically, RTC clock source is 32 kHz LPO clock.

6.2 Switching specifications

6.2.1 Control timing

Table 6-4 Control timing

Num	C	Rating		Symbol	Min.	Typ. [1]	Max.	Unit
1	D	System and core clock (t_{sys} = 1/f_{Sys})		f_{Sys}	DC	—	32	MHz
2	P	Bus frequency (t_{cyc} = 1/f_{Bus})		f_{Bus}	DC	—	32[2]	MHz
3	P	Internal low power oscillator frequency		f_{LPO}	—	32	—	kHz
4	D	External reset pulse width [3]		t_{extrst}	1.5 ×t32k	—	—	ns
5	D	IRQ pulse width	Run mode [4]	t_{ILIH}/ t_{IHIL}	1.5 × t_{sys}	—	—	ns
	D		Stop mode [4]	t_{ILIH}/ t_{IHIL}	1.5 × t_{32k}	—	—	ns
6	D	Port rise and fall time - Normal drive strength(load = 50 pF) [5]	—	t_{Rise}	—	10.2	—	ns
	D			t_{Fall}	—	9.5	—	ns
	D	Port rise and fall time - high drive strength(load = 50 pF) [5]	—	t_{Rise}	—	5.4	—	ns
	D			t_{Fall}	—	4.6	—	ns

[1] Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

[2] The maximum operating frequency of AC7801x series, please refer to the product selection table.

[3] This is the shortest pulse that is guaranteed to be recognized as a RESET_B pin request.

[4] This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized.

[5] Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature ranges -40 °C to 125 °C.

6.2.2 PWM module timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the PWM clock.

Table 6-5 PWM input timing

C	Function	Symbol	Min.	Max.	Unit
D	Timer clock frequency	f_{PWM}	—	16M	Hz
D	Input capture pulse width	t_{ICPW}	1.5	—	tPWM [1]

[1] $t_{PWM} = 1/f_{PWM}$

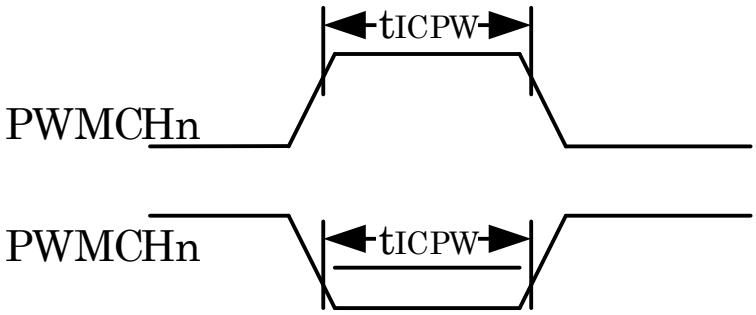


Figure 6-2 Timer input capture pulse

6.3 Thermal specifications

6.3.1 Thermal characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user- determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 6-6 Thermal characteristics

Board type	Symbol	Description	32 HVQFN	20 TSSOP	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	37.36	51.55	°C/W	1, 2

Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	17.59	34.36	°C/W	1, 3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	31.11	45.38	°C/W	1, 3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	13.72	30.44	°C/W	1, 3
Single-layer (1s)	$R_{\theta JB}$	Thermal resistance, junction to board	7.90	21.71	°C/W	4
Four-layer (2s2p)	$R_{\theta JB}$	Thermal resistance, junction to board	5.19	21.56	°C/W	4
Single-layer (1s)	$R_{\theta JC}$	Thermal resistance, junction to case	27.08	27.67	°C/W	5
Four-layer (2s2p)	$R_{\theta JC}$	Thermal resistance, junction to case	27.08	27.67	°C/W	5
Single-layer (1s)	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center(natural convection)	0.50	0.41	°C/W	6
Four-layer (2s2p)	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center(natural convection)	0.35	0.30	°C/W	6
Single-layer (1s)	Ψ_{JB}	Thermal characterization parameter, junction to package bottom outside center(natural convection)	7.75	21.51	°C/W	7
Four-layer (2s2p)	Ψ_{JB}	Thermal characterization parameter, junction to package bottom outside center(natural convection)	5.17	21.47	°C/W	7

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
3. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board

meets JESD51-9 specification for 1s or 2s2p board, respectively.

4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

The average chip-junction temperature (T_J) in °C can be obtained from:

$T_J = T_A + (P_D \times \theta_{JA})$ Where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts - chip internal power

$P_{I/O}$ = Power dissipation on input and output pins - user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$P_D = K \div (T_J + 273\ °C)$

Solving the equations above for K gives: $K = P_D \times (T_A + 273\ °C) + \theta_{JA} \times (PD)^2$

where K is a constant pertaining to the particular part. K can be determined by measuring

P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving the above equations iteratively for any value of T_A.

7 Peripheral operating requirements and behaviors

7.1 Core modules

7.1.1 SWD electricals

Table 7-1 SWD full voltage range electrical

Symbol	Description	Min.	Max.	Unit
—	Operating voltage	2.7	5.5	V
J1	SWD_CLK frequency of operation • Serial wire debug	0	20	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	5	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	5	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	42	ns

7.2 External oscillator (OSC) and ICS characteristics

7.2.1 External oscillator(OSC) characteristics

Table 7-2 OSC specifications (temperature range = -40 to 125 °C ambient)

Num	C	Characteristic	Symbol	Min.	Typ.	Max.	Unit
1	C	Crystal frequency	f_{hi}	8	—	20	MHz
2	D	Load capacitors	C_{L1}, C_{L2}	See Note [1]			
3	D	Series resistor	RS	—	0	—	KΩ
4	C	Crystal start-up time	t_{CST}	—	—	2.5	ms

[1] For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors designed for high-frequency applications, and selected to match the requirements of the crystal. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

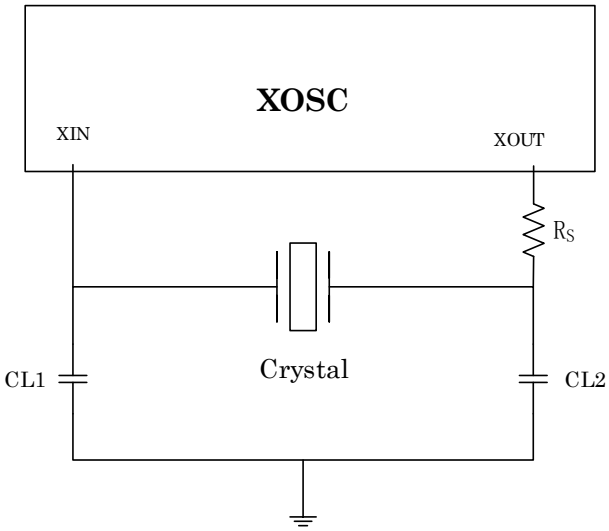


Figure 7-1 Typical crystal or resonator circuit

7.2.2 Internal RC characteristics

Table 7-3 OSC and ICS specifications (temperature range = -40 to 125 °C ambient)

Num	C	Characteristic		Symbol	Min.	Typ.	Max.	Unit
1	P	LFOSC output frequency range	Over temperature range from -40 °C to 125°C	f_{lfosc}	31.52	32	32.48	MHz
2	P	LPOSC Internal reference clock frequency, factory trimmed	T = 25 °C, V_{DD} = 5 V	f_{int_ft}	—	32	—	KHz
3	P	LPOSC Factory trimmed internal oscillator accuracy	T = 25 °C, V_{DD} = 5 V	Δ_{fint_ft}	-2	—	2	%
4	P	LPOSC Deviation of IRC over temperature when trimmed at T = 25 °C, V_{DD} = 2.7-5.5 V	Over temperature range from -40 °C to 125°C	Δ_{fint_t}	-10	—	10	%

7.3 Embedded Flash specifications

This section provides details about program/erase/read parameters and reliability features for the Flash memory.

Table 7-4 Flash characteristics

C	Characteristic	Symbol	Min.	Typ.	Max.	Unit
D	Supply voltage for program/erase at temperature from - 40°C to 125 °C	$V_{prog/erase}$	2.7	—	5.5	V
D	Supply voltage for read operation at temperature from	V_{Read}	2.7	—	5.5	V
D	Flash Bus frequency	f_{SYS}	8	32	32	MHz
D	Mass Erase (all Main Block pages)	t_{MER}	—	23	—	ms
D	Page Erase (one page)	t_{PER}	—	5	—	ms
D	Mass Erase Verify	t_{MERV}	—	32774	—	t_{cyc} [1]
D	Page Erase Verify	t_{PERV}	—	262(128word)	—	t_{cyc} [1]
D	Program Flash (1 word)	t_{PRG1}	—	46.6	—	us
D	Program Flash (n word, n>1)	t_{PRGn}	—	46.6+24.5×(n-1)		us
C	Flash Program/erase endurance at temperature from - 40°C to 125 °C	n_{EDR}	10 k	—	—	times
C	Data retention at an average junction temperature of TJavg = 85°C after up to 10,000 program/erase cycles	t_{RET}	100@25 20@105 10@125℃	—	—	year

[1] t_{cyc} = 1/ f_{SYS}.

7.4 Analog

7.4.1 ADC and Tsensor characteristics

Table 7-5 12 bit ADC and Tsensor Operating Conditions and Characteristics

C	Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
D	V_{AVDD}	Supply Voltage	Absolute	2.7	—	5.5	V
D	V_{REFH}	Positive reference input	Absolute	2.5		V_{AVDD}+0.1	V
D	V_{REFL}	Negative reference input	Absolute	—	0	—	V
D		Input Voltage Range	Refer to the Supply Power	0	—	V_{AVDD}	**V**
	V_{IN}		Refer to the V_{REFH}	0	—	V_{REFH}	**V**

C	Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
D	R_{IN}	Source impedance	—	—	—	—	Ω
D	C_{ADC}	Internal Sampling Capacitor	—	—	2.064	—	pF
D	R_{ADC}	Sampling switch resistance	—	—	2.5	—	KΩ
D	f_{ADC}	ADC Clock Frequency	—	—	—	16	MHz
D	f_{sample}	Sampling Time	—	2.125	—	—	us
C	frate	Conversion Rate	f_{ADC}=24 MHz	—	—	0.25	MHz
C	INL	Integral Non-Linearity	—	—	1.5	—	LSB [2]
C	DNL	Differential Non-Linearity	—	—	1.5	—	LSB [2]
P	CH	External Channels	—	—	—	19	—

[1] $R_{IN} < \frac{N_{sample}}{f_{ADC} * C_{ADC} * ln(2^{N+2})} - R_{ADC}$

[2] LSB = V_{AVDD} /2^{12}

Table 7-6 12 bit ADC and Tsensor Operating Conditions and Characteristics(continue)

Characteristic	Conditions	C	Symbol	Min.	Typ.	Max.	Unit
Temp sensor slope	-40 °C~125 °C	D	Slope	—	-1.709	—	mV/°C
Temp sensor voltage	25 °C	D	V_{TEMP25}	—	0.705	—	V

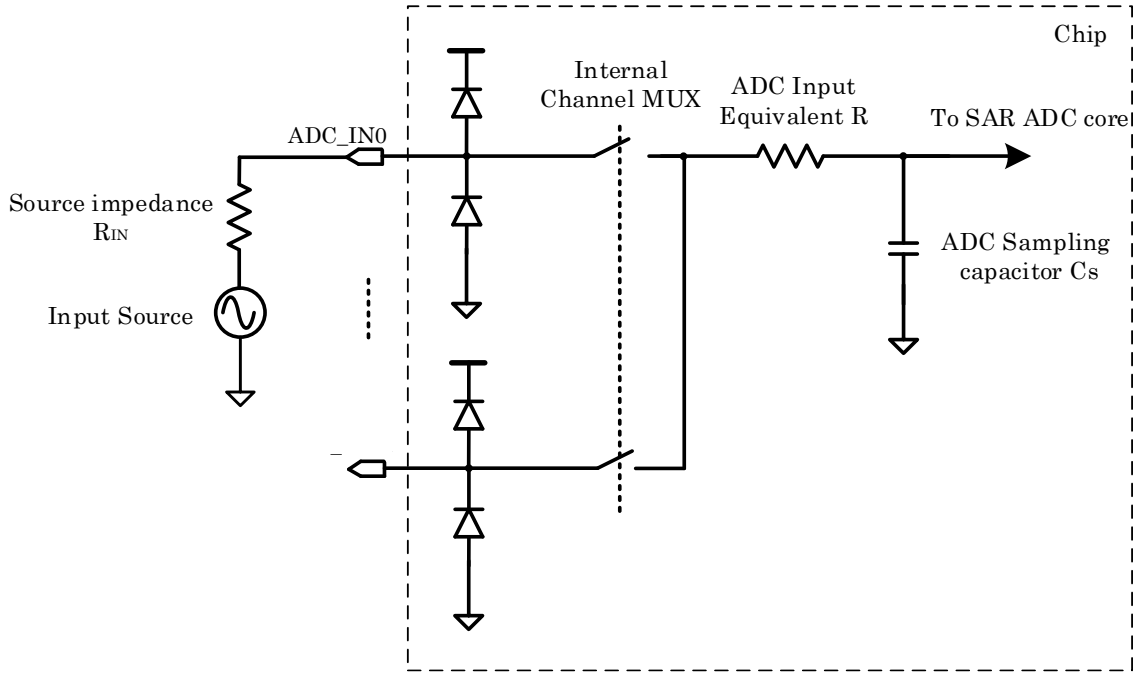


Figure 7-2 ADC input equivalent diagram

7.4.2 Analog comparator (ACMP) electricals

Table 7-7 Comparator electrical specifications

C	Characteristic	Condition	Symbol	Min.	Typ.	Max.	Unit
D	Supply voltage	—	V_{AVDD}	2.5	—	5.5	V
T	Supply current	Only ACMP	I_{DDA}	—	—	20	μA
D	Analog input voltage	—	V_{AIN}	V_{SS}	—	V_{AVDD}	V
P	Analog input offset	—	V_{AIO}	-30	—	30	mV
C	Analog comparator hysteresis voltage	No hysteresis	V_{HYS}	—	0	—	mV
C	Analog comparator hysteresis voltage (HYST=0)	low hysteresis	V_{HYS}	—	10	—	mV
C	Analog comparator hysteresis voltage (HYST=0)	Middle hysteresis	V_{HYS}	—	20	—	mV
C	Analog comparator hysteresis voltage (HYST=0)	high hysteresis	V_{HYS}	—	40	—	mV
D	Supply current (off mode)	—	I_{DDAOFF}	—	—	100	nA
T	Propagation delay	—	t_D	—	0.4	1[1]	μs

P	Digital-to-analog converter integration nonlinearity	Vref=V_{AVDD}	INL	TBD	—	TBD	LSB
P	Digital-to-analog converter integration nonlinearity	Vref=V_{BG}	INL	TBD	—	TBD	LSB
T	Digital-to-analog converter output	With buffer	DAC_OUT	0.2		V_{AVDD} -0.2	V
T	Digital-to-analog converter output	Without buffer	DAC_OUT	TBD	—	TBD	V
D	Digital-to-analog converter load capacitance	—	C_{LOAD}	—	6	—	pF
D	Digital-to-analog converter static power consumption	Vref=5.5V	I_{DDA}	—	10	—	μA
D	Digital-to-analog converter static power consumption	Vref=V_{BG}	I_{DDA}	—	20	—	μA
D	Digital-to-analog converter buffer static power dissipation	—	I_{DDA}	—	25	—	μA

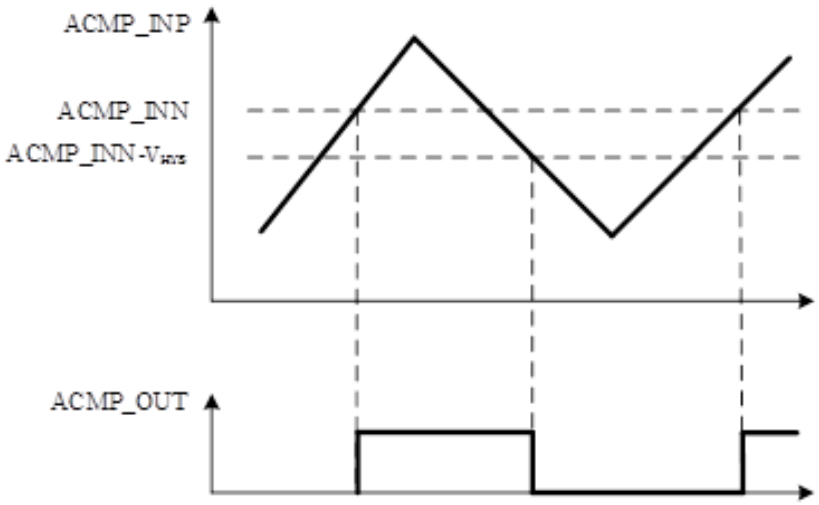


Figure 7-3 ACMP hysteresis diagram

[1] Input of ACMP use external channel, low-pass-filter choose 2M Hz

7.5 Communication interfaces

7.5.1 SPI specifications

The serial peripheral interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's reference manual for information about the modified transfer formats used for communicating with slower peripheral devices. All timing is shown with respect to 20% V_{DD} and 80% V_{DD}, unless noted. All timing assumes slew rate control is disabled and high-drive strength is enabled for SPI output pins.

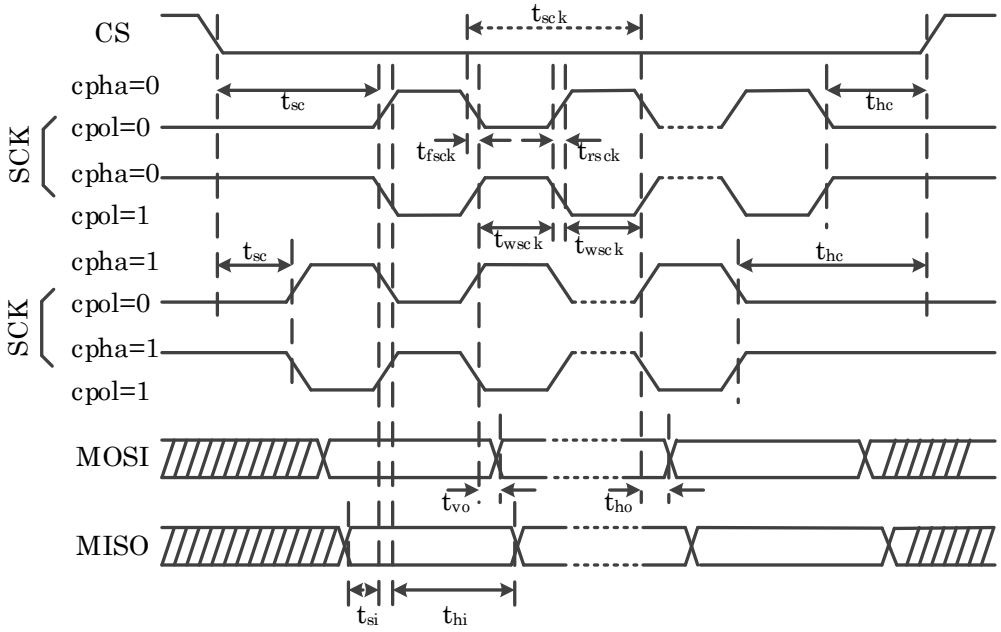


Figure 7-4 SPI timing diagram – master

Table 7-8 SPI characteristics – master

Symbol	Description	Min.	Max.	Unit	Comment
f_{op}	Frequency of operation	f_{bus}/512	f_{bus}/2	Hz	f_{bus} is bus clock,the max is 16Mhz
t_{sc}	CS setup time	1×t_{bus}	256×t_{bus}	ns	Negative edge of CS to first SCK edge
t_{hc}	CS hold time	1×t_{bus}	256×t_{bus}	ns	Last SCK edge to positive edge of CS
t_{wsck}	SCK high or low level time	1×t_{bus}	256×t_{bus}	ns	No considering **t_{rsck}** and **t_{fsck}**
t_{si}	Data input setup time	10	—	ns	—
t_{hi}	Data input hold time	25	—	ns	—
t_{vo}	Data output valid time	—	5	ns	—

Symbol	Description	Min.	Max.	Unit	Comment
t_{ho}	Data output hold time	1	—	ns	—

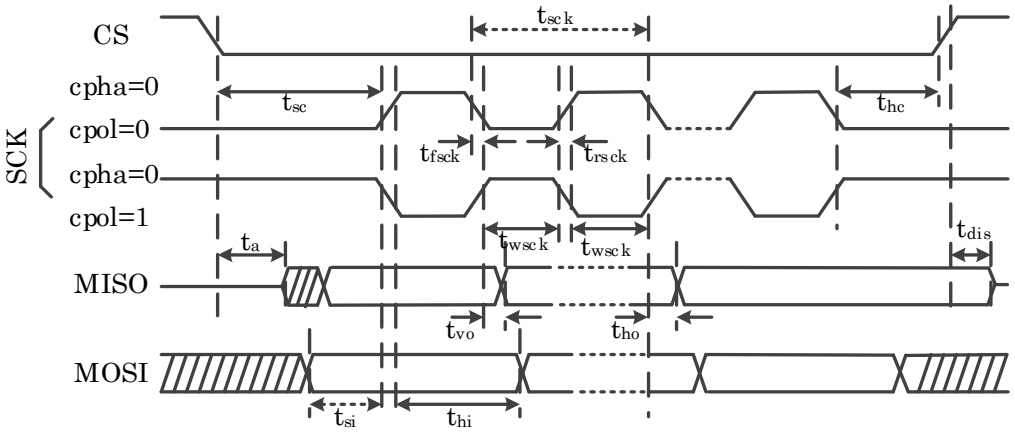


Figure 7-5 SPI timing diagram – slave(cpha=0)

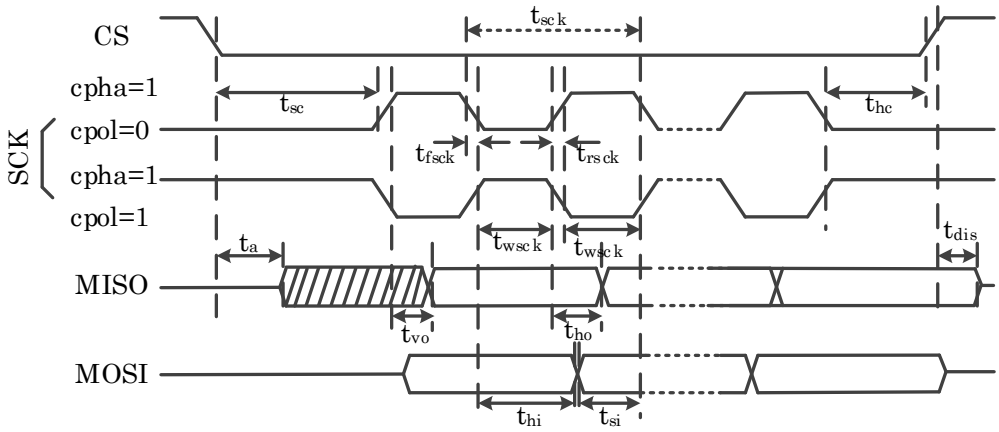


Figure 7-6 SPI timing diagram – slave(cpha=1)

Table 7-9 SPI characteristics - slave

Symbol	Description	Min.	Max.	Unit	Comment
f_{op}	Frequency of operation	-	8 M	Hz	Polling reception mode, up to 8M; Interrupt reception mode, up to 1M (affected by CPU processing power and user interrupt callback function efficiency)
t_{sc}	CS setup time	$2\times t_{bus}$	—	ns	Negative edge of CS to first SCK edge
t_{hc}	CS hold time	$2\times t_{bus}$	—	ns	Last SCK edge to positive edge of CS

Symbol	Description	Min.	Max.	Unit	Comment
t_a	slave access time	—	t_{bus}	ns	Data from "Z" to effective
t_{dis}	slave MISO disable time	—	t_{bus}	ns	Data from effective to "Z"
t_{si}	Data input setup time	50	—	ns	—
t_{hi}	Data input hold time	35	—	ns	—
t_{vo}	Data output valid time	—	35	ns	—
t_{ho}	Data output hold time	10	-	ns	—

7.5.2 UART specifications

Basic function of Universal Asynchronous Receiver/Transmitter (UART) is to transmit and receive the serial data bit by bit. In order to support transmitting break field, sync field and data, additional Soft Local Interconnect Network(LIN) is included in the AC7802x chips. The main parameters of UART is introduced as below:

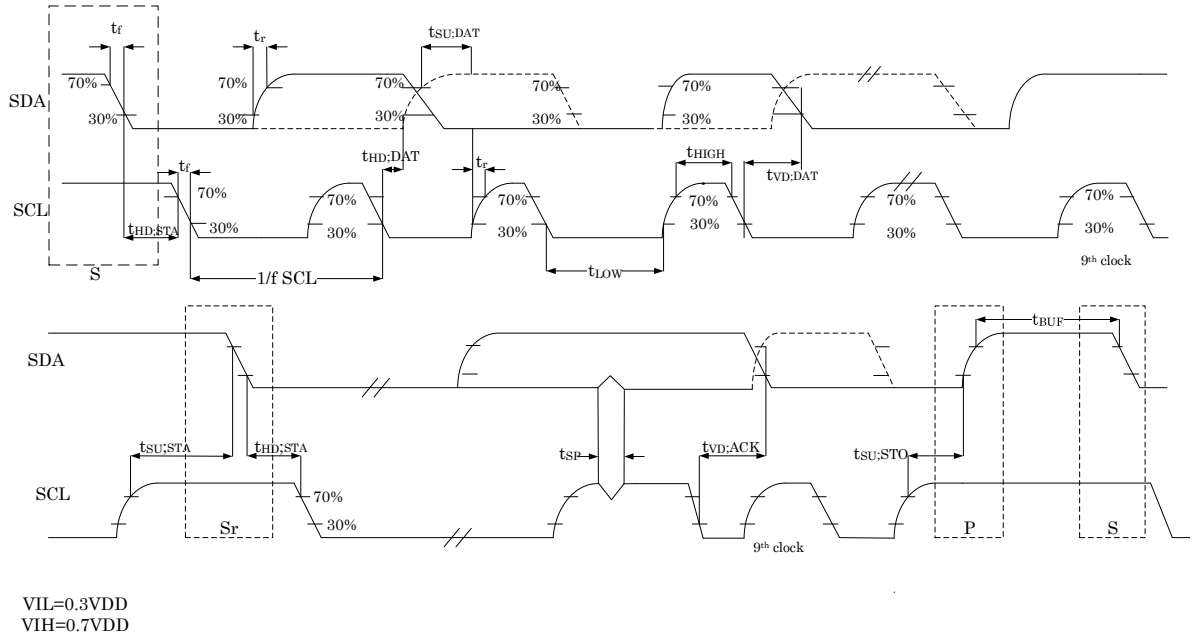
1. Two UART function channels and one of which support soft LIN functions (the uart function and LIN function of the same UART cannot be used at the same time).
2. UART can transmit or receive data with the range of baud rate from 600 bps to 4Mbps.when receive data, In the polling mode, the baud rate supports up to 4M bps, and the interrupt mode, the baud rate supports up to 2M bps (affected by the CPU processing capacity and the efficiency of the user's interrupt callback function);
3. The minimum GPIO pin interrupt pulse width is 333 ns. Because of that these pins do not have a passive filter on the inputs, this is the shortest pulse width that is guaranteed to be recognized.
4. The maximum baud rate supported in soft LIN function is 20 kbps.
5. Auto baud rate detection is selectable open or not in soft LIN function. The tolerance of received baud rate is from -50%to +100% .

7.5.3 I2C specifications

Table 7-10 Characteristics of the I2C bus lines for different mode

Symbol	Parameter	Standard-mode		Fast-mode		Fast-mode Plus		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCL}	SCL clock frequency	0	100	0	400	0	1000	kHz
$t_{HD;STA}$	hold time (repeated) START condition	4	—	0.6	—	0.26	—	μs

t_{LOW}	LOW period of the SCL clock	4.7	—	1.3	—	0.5	—	µs
t_{HIGH}	HIGH period of the SCL clock	4	—	0.6	—	0.26	—	µs
$t_{SU;STA}$	set-up time for a repeated START condition	4.7	—	0.6	—	0.26	—	µs
$t_{HD;DAT}$	data hold time	0	—	0	—	0	—	µs
$t_{SU;DAT}$	data set-up time	250	—	100	—	50	—	ns
t_r	rise time of both SDA and SCL signals	—	1000	20	300	—	120	ns
t_f	fall time of both SDA and SCL signals set-up time for STOP condition	—	300	20 × (V_{DD} / 5.5 V)	300	20 × (V_{DD} / 5.5 V)	120	ns
$t_{SU;STO}$	bus free time between a STOP and START condition	4	—	0.6	—	0.26	—	µs
t_{BUF}	capacitive load for each bus line	4.7	—	1.3	—	0.5	—	µs
C_b	data valid time	—	400	—	400	—	550	pF
$t_{VD;DAT}$	data valid acknowledge time	—	3.45	—	0.9	—	0.45	µs
$t_{VD;ACK}$	noise margin at the LOW level	—	3.45	-	0.9	-	0.45	µs
V_{nL}	noise margin at the HIGH level	$0.1V_{DD}$	—	$0.1V_{DD}$	—	$0.1V_{DD}$	—	V
V_{nH}	SCL clock frequency	$0.2V_{DD}$	—	$0.2V_{DD}$	—	$0.2V_{DD}$	—	V



VIL=0.3VDD
VIH=0.7VDD

Figure 7-7 Definition of timing for F/S-mode devices on the I2C-bus

8 Dimensions

8.1 HVQFN32 package information

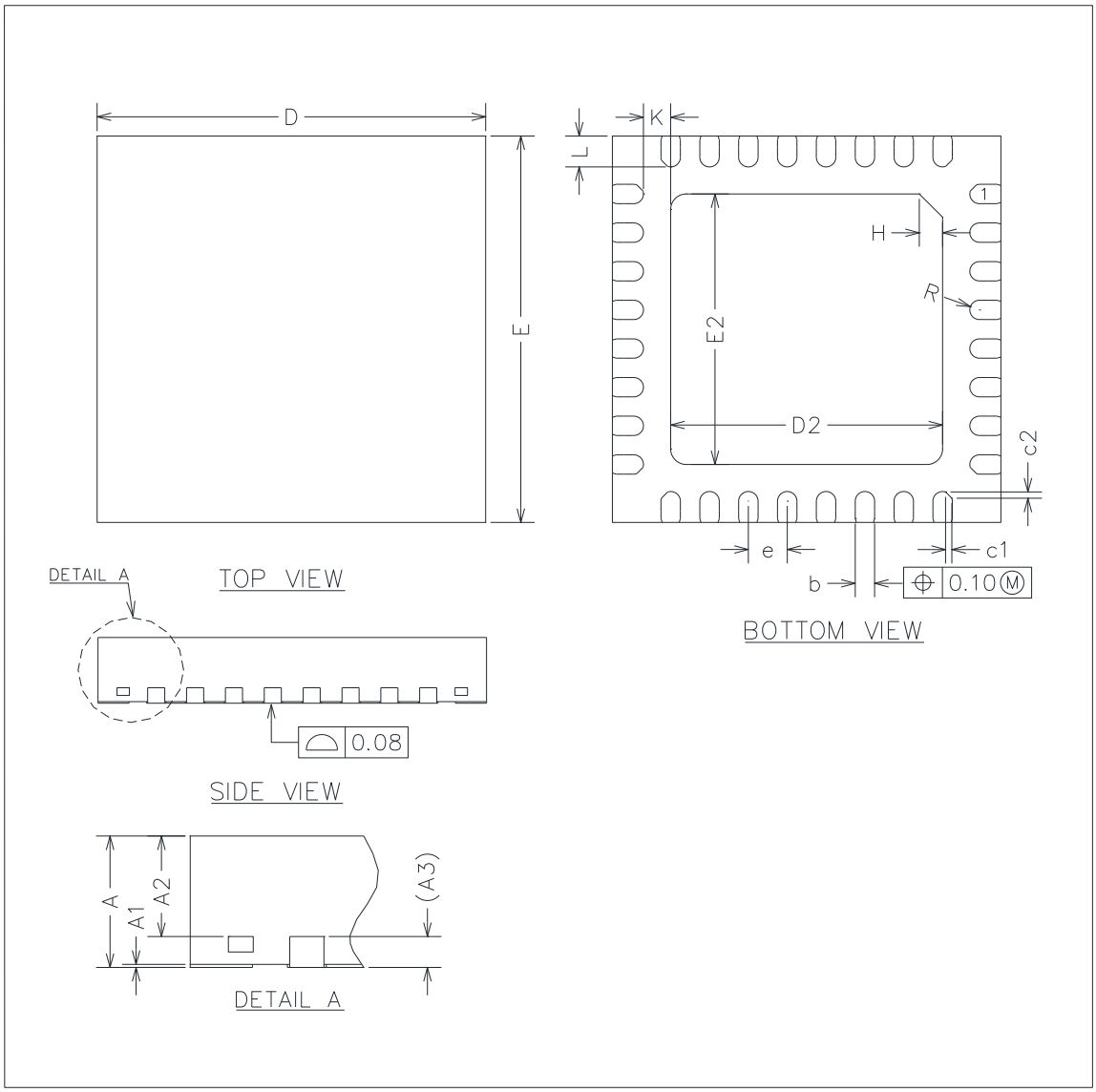


Figure 8-1 HVQFN32 - 32-pin, 5 x 5 mm thermal enhanced very thin quad flat no-lead package outline [1]

[1] Drawing is not to scale.

Table 8-1 HVQFN 32 - 32-pin, 5 x 5 mm thermal enhanced very thin quad flat no-lead package mechanical data [1]

ITEM		SYMBOL	Min.	NOM.	Max.
Total height		A	0.80	0.85	0.90
Stand off		A1	0	0.02	0.05
Leadframe to mold height		A2	0.60	0.65	0.70
Leadframe thickness		A3	0.20REF		
Lead width		b	0.20	0.25	0.30
Package size	X	D	4.90	5.00	5.10
	Y	E	4.90	5.00	5.10
Exposed pad size	X	D2	3.40	3.50	3.60
	Y	E2	3.40	3.50	3.60
Lead pitch		e	0.40	0.50	0.60
PIN1 logo size of exposed pad		H	0.30REF		
Distance between pin and exposed pad		K	0.35REF		
Lead length		L	0.35	0.40	0.45
R		R	0.09	—	—
c1		c1	—	0.08	—
c2		c2	—	0.08	—

[1] Dimensions are expressed in millimeters.

Device Marking for HVQFN32

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

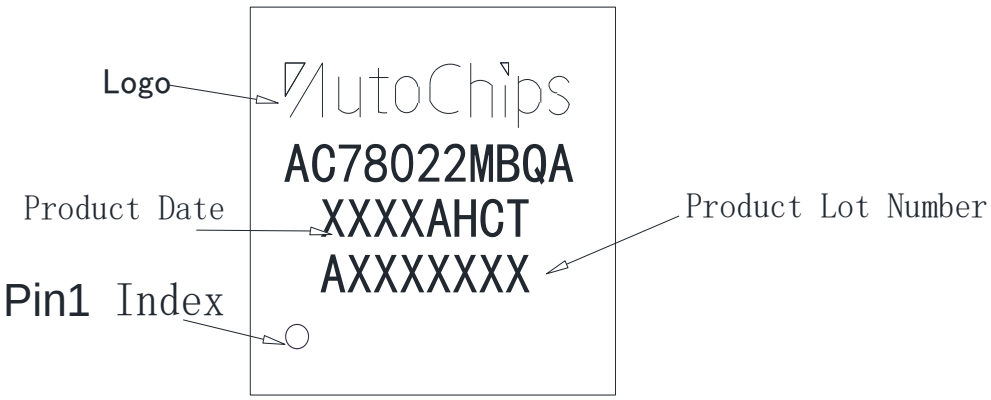


Figure 8-2 HVQFN32 marking example (package top view)

8.2 TSSOP20 package information

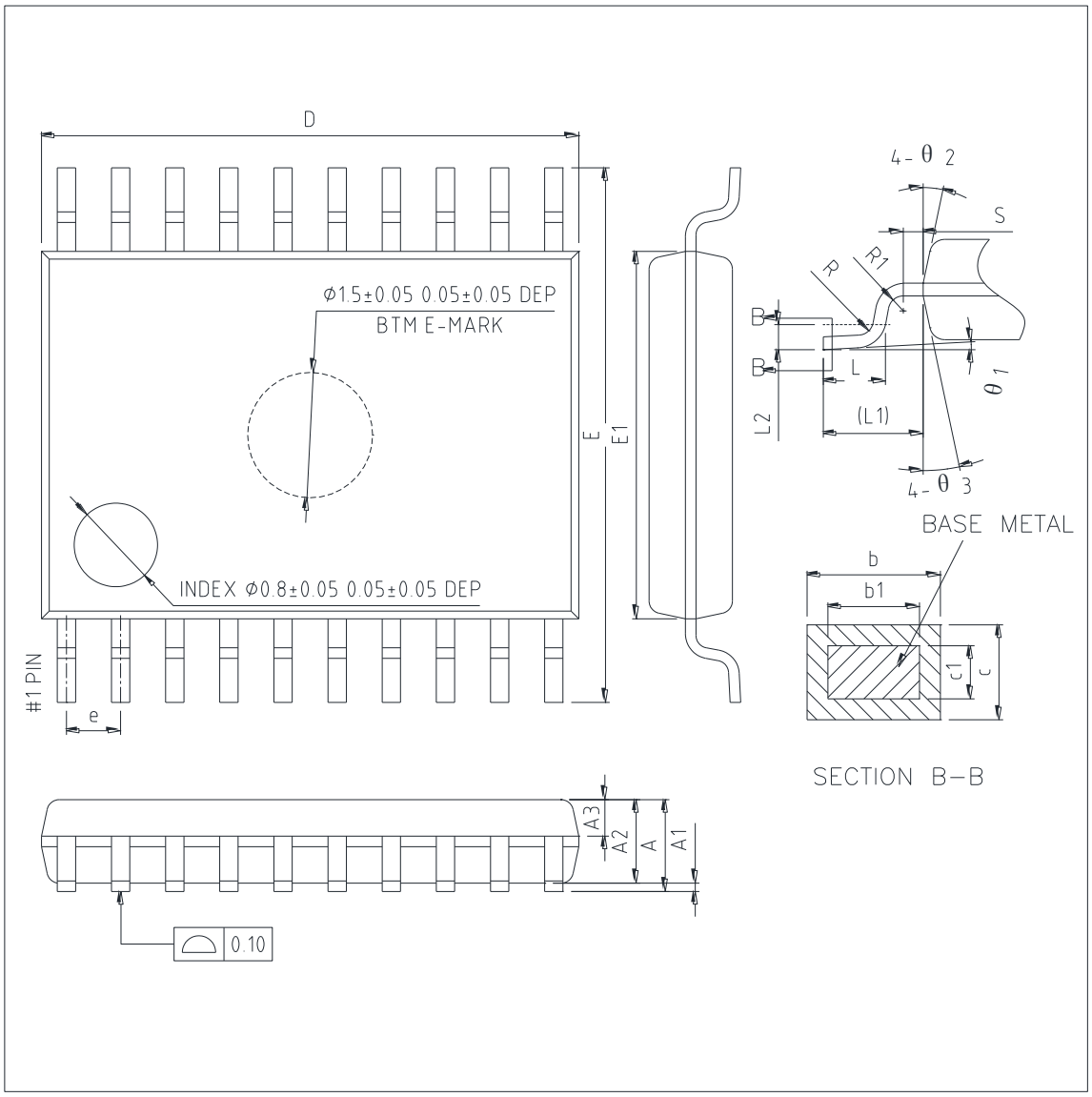


Figure 8-3 TSSOP20 – 20 pin, 6.5 x 4.4 mm thin shrink small outline package outline [1]

[1] Drawing is not to scale.

Table 8-2 TSSOP20 – 20 pin, 6.5 x 4.4 mm thin shrink small outline package mechanical data [1]

ITEM		SYMBOL	Min.	NOM.	Max.
Total height		A	—	—	1.20
Stand off		A1	0.05	—	0.15
Mold thickness		A2	0.90	1.00	1.05
Leadframe to mold height		A3	0.34	0.44	0.54
Lead width		b	0.20	—	0.28
Lead width without plating		b1	0.20	0.22	0.24
Lead frame thickness		c	0.10	—	0.19
Lead frame thickness without plating		c1	0.10	0.13	0.15
Outer Lead Distance Package size	Y	E	6.20	6.40	6.60
Package size	X	D	6.40	6.50	6.60
	Y	E1	4.30	4.40	4.50
Lead pitch	e	0.55	0.55	0.65	0.75
L		L	0.45	0.60	0.75
Lead length		L1	1.00 REF		
L2		L2	0.25 BSC		
R		R	0.09	—	—
R1		R1	0.09	—	—
S		S	0.20	—	—
Angle 1		Θ	0°	—	8°
Angle 2		Θ1	10°	12°	14°
Angle 3		Θ2	10°	12°	14°

[1] Dimensions are expressed in millimeters.

Device Marking for TSSOP20

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

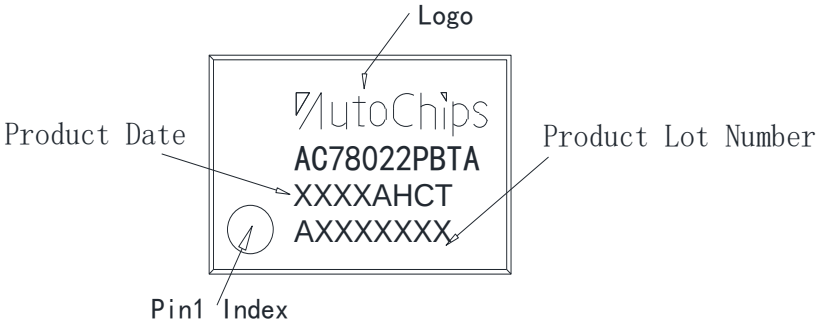


Figure 8-4 TSSOP20 marking example (package top view)

9 Pinout

9.1 Signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

Table 9-1 Signal multiplexing and pin assignments [2]

32 PIN HVQFN	20 PIN TSSOP	Pin Name	Function 0	Function 1	Function 2	Function 3	PINMUX	GPIO
1		PB0	gpio	ADC_IN18	PWM1_CH1	PWM2_FLT1	PMUX1[20:18]	16
2		PB1	gpio		PWM1_CH0	DAC_OUT	PMUX1[23:21]	17
3	4	VDD1						
4	5	VSS1						
5	6	PA12	gpio	I2C0_SCL	OSC_OUT[1]	PWM0_FLT0	PMUX1[8:6]	12
6	7	PA15	gpio	I2C0_SDA	OSC_IN[1]	PWDT0_IN0	PMUX1[17:15]	15
7	8	PA0	gpio	PWM2_CH3	VREF-/ADC_IN10	I2C0_SCL	PMUX0[2:0]	0
8	9	PA1	gpio	PWM2_CH2	VREF+/ADC_IN9	I2C0_SDA	PMUX0[5:3]	1
9		PB3	gpio	PWM2_CH0	ADC_IN13	SPI0_MOSI	PMUX1[29:27]	19
10	10	PA2	gpio	PWM2_CH1	ADC_IN8	SPI0_MISO	PMUX0[8:6]	2
11	11	PA3	gpio	PWM2_CH0	ADC_IN7	SPI0_SCK	PMUX0[11:9]	3
12	12	PA4	gpio	PWM0_CH1	ADC_IN6/ACMP_IN6	UART1_TX	PMUX0[14:12]	4
13	13	PA5	gpio	PWM0_CH0	ADC_IN5/ACMP_IN5	UART1_RX	PMUX0[17:15]	5
14	14	PA6	gpio	BOOT[1]	gpio	SPI0_NSS	PMUX0[20:18]	6
15		PB4	gpio	PWM2_CH1	ADC_IN12	SPI0_MISO	PMUX2[2:0]	20
16		PB5	gpio	PWM0_CH0	ADC_IN11	SPI0_SCK	PMUX2[5:3]	21
17	15	PA7	gpio	UART0_TX	ADC_IN4/ACMP_IN4	SPI0_MOSI	PMUX0[23:21]	7
18	16	PA8	gpio	UART0_RX	ADC_IN3/ACMP_IN3	SPI0_NSS	PMUX0[26:24]	8
19	17	PA9	gpio	PWM2_FLT0	ADC_IN2/ACMP_IN2	RTC_CLKIN	PMUX0[29:27]	9
20		VSS2						
21	18	VDD2						
22		PB6	gpio	ADC_IN16	PWM1_FLT0	PWM0_FLT1	PMUX2[8:6]	22
23		PB7	gpio	ADC_IN15	ACMP_IN7	I2C0_SCL	PMUX2[11:9]	23
24		PB8	gpio	ADC_IN14	PWDT0_IN2	I2C0_SDA	PMUX2[14:12]	24
25	19	PA10	gpio	PWM1_CH1	ADC_IN1/ACMP_IN1	PWDT0_IN2	PMUX1[2:0]	10
26	20	PA11	gpio	PWM1_CH0	ADC_IN0/ACMP_IN0	PWDT0_IN1	PMUX1[5:3]	11
27		PB9	gpio	PWM2_CH3	I2C0_SCL	UART0_TX	PMUX2[17:15]	25
28		PB10	gpio	PWM2_CH2	I2C0_SDA	UART0_RX	PMUX2[20:18]	26
29		PB2	gpio	NMI_B	PWM1_FLT1	PWDT0_IN0	PMUX1[26:24]	18
30	1	PA13	gpio	SWD_CLK[1]	EXT_CLKIN	RTC_CLKOUT	PMUX1[11:9]	13
31	2	RESET_B	RESET_B					
32	3	PA14	gpio	SWD_DIO[1]	ACMP_OUT	PWM0_CH1	PMUX1[14:12]	14

[1] This functions as default function.

[2] All the pins are default as gpio on the first time power on except some dedicated pins.

For example, if we want to configure PIN1(PB11) as PWM0_CH3, we should set PMUX2[23:21] = 1.

9.2 Device pin assignment

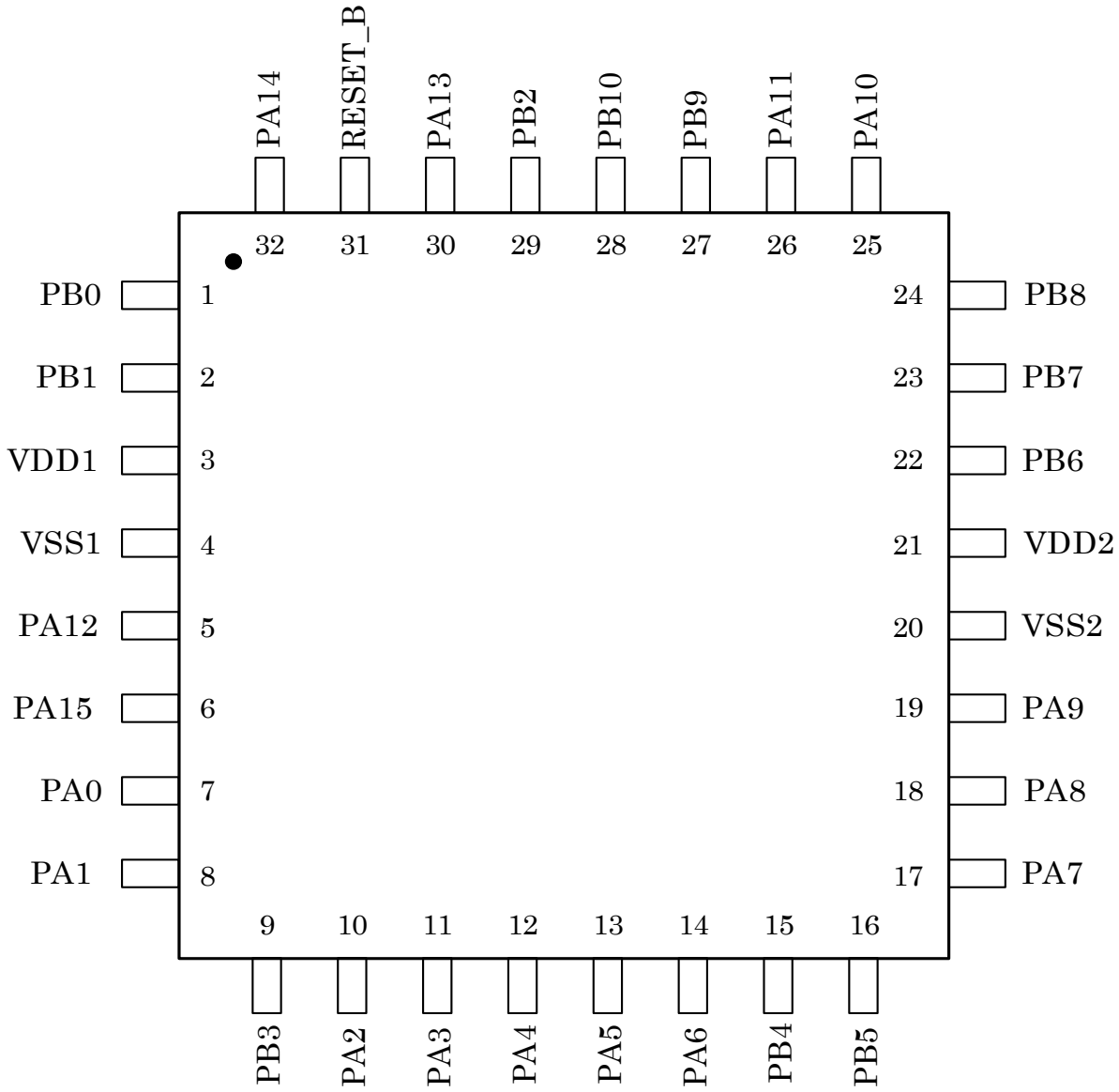


Figure 9-1 32-pin HVQFN32 package

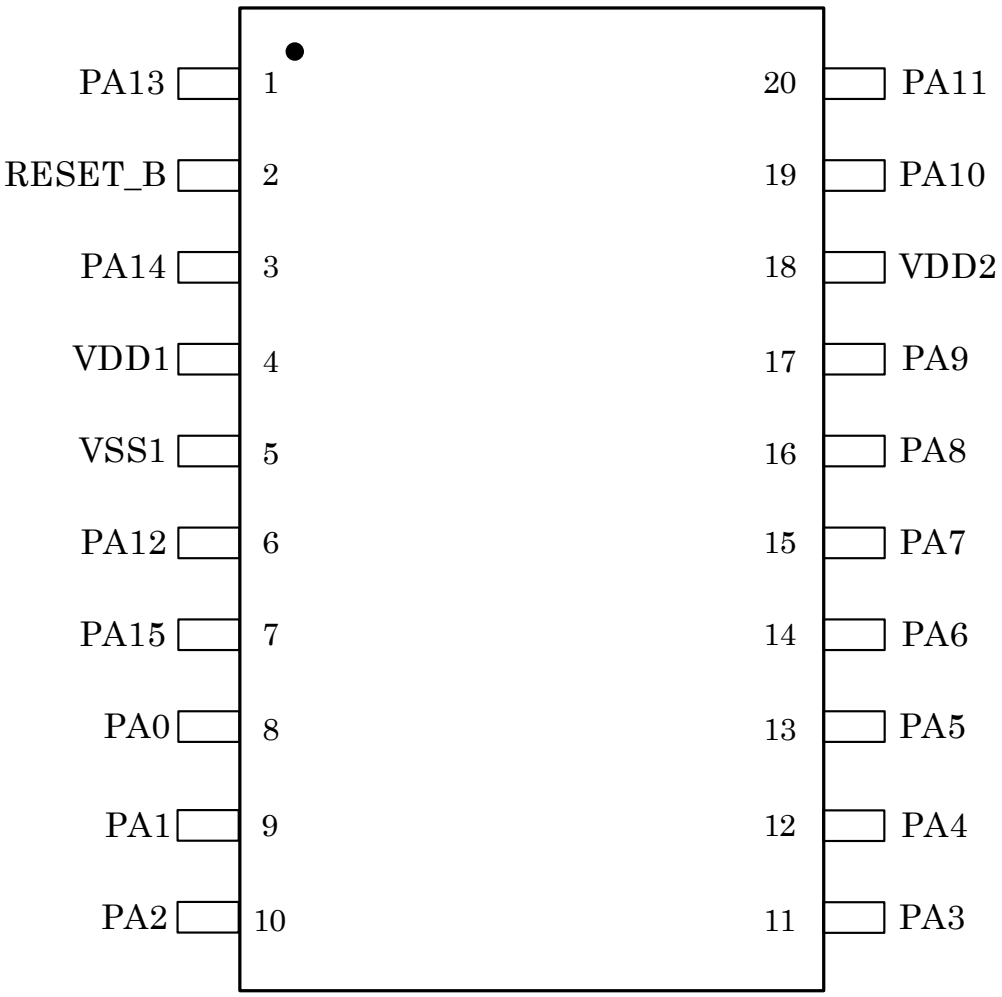


Figure 9-2 20-pin TSSOP20 package