AC7801L Data Sheet

Supports the following:

AC7801LFDEA, AC7801LFCEA

Version: 1.5

Release date: 2025-04-08

Document Revision History

Revision	Date	Author	Description
1.0	2024-03-04	AutoChips	Initial version
1.1	2024-04-10	AutoChips	Modify AC7801L PINMUX and related content
1.2	2024-04-28	AutoChips	Modify standby mode description
1.3	2024-06-11	AutoChips	Modify the document format and some parameters
1.4	2024-10-11	AutoChips	Modify parameters
1.5	2025-04-08	AutoChips	Modify parameters

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1 Key features

- Automotive grade
  - AEC-Q100 Grade 1 qualified
- Performance
  - Up to 48 MHz ARM® Cortex-M0+ core
  - Single cycle 32-bit multiplier
  - Fast I/O access port
  - Hardware coprocessor (Memory-Mapped Division and Square Root)
- Memories and memory interfaces
  - Up to 128 KB Flash
  - 20 KB SRAM, ECC is supported
- Clocks
  - Oscillator (OSC) - supports 4 MHz to 30 MHz crystal or ceramic resonator; choice of low power or high gain oscillators
  - System PLL - Internal PLL, supports internal or external reference clock source, can generate up to 48MHz system clock
  - Internal clock source (LFOSC) – Internal RC oscillator provides 8MHz clock source
  - Internal 32 kHz low-power oscillator (LPO)
- System peripherals
  - Power management module (PMC) with three power modes: Run, Wait, Stop
  - Low-voltage detection (LVD) with reset
  - Watchdog with independent clock source(WDOG)
  - Programmable cyclic redundancy check module(CRC)
  - Serial wire debug (SWD) interfaces
  - One 4-channel DMA
- Human-machine interface
  - Up to 33 general-purpose input/output (GPIO)
  - External interrupt (IRQ)
- Analog modules
  - One up to 12-channel 12-bit 1Msps SAR ADC, optional hardware trigger (ADC)
  - One analog comparators containing a 6-bit DAC and programmable reference input(ACMP)
  - Integrated high-voltage LDO, 5.5V~28V input, 5V output, 70mA
  - Integrated LIN PHY transceiver, supports 12V applications, supports ±40V LIN bus fault tolerance, 40V load dump

- Timers
  - Two 8-channel PWM
    (PWM1_CH1 is used internally)
  - One 4-channel periodic interrupt timer (TIMER)
  - Two pulse width timer (PWDT)
  - One real-time clock (RTC)

- Operating characteristics
  - Voltage range: 5.5 V to 28 V
  - Temperature range (ambient):
    -40°C to 125°C

- Package options
  - 48-pin LQFP-EP

- Communication interfaces
  - One CAN-FD module, compatible with CAN
  - Three UART modules (two support Software LIN, The internal LIN transceiver occupies 1 channel)
  - Two SPI modules (SPI)
  - Two I2C modules (I2C)

2 Block diagram

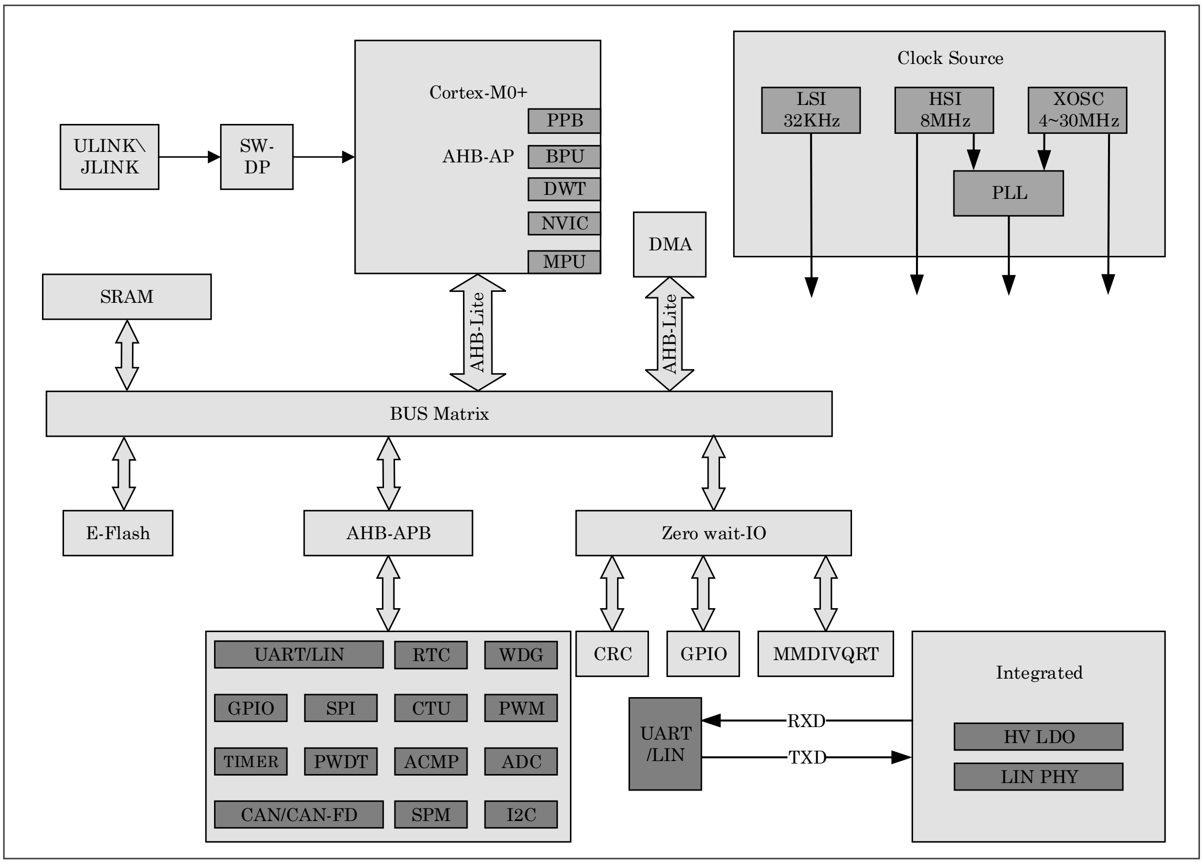

Figure 2-1 AC7801L Block Diagram

3 Part identification

3.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

3.2 Format

Part numbers for this device have the following format:

AC## GTUFPN

3.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Table 3-1 Fields

Field	Description	Values
AC	Autochips	• AC
7	AutoChips MCU family	• 7
8	General Purpose Automotive MCU	• 8
0	Core Platform	• 0= Cortex-M0+
1	Specific Function Bit	• 1 = performance/version bit
L		• L = Product subfamily L: Integrated LIN PHY and LDO C: Integrated CAN PHY and LDO H: Integrated HS/LS, LIN PHY and LDO B: Integrated Bridge-driver, CAN/LIN PHY and LDO P: Integrated Pre-driver, CAN/LIN PHY and LDO
F	Pin Count	• P = 20 • M = 32 • F = 48 • J = 56 • H = 64 • S = 80 • L = 100
D	Flash Memory Size	• A = 16 KB • B = 32 KB • C = 64 KB • D = 128 KB
E	Package type	• L = LQFP • Q = QFN • T = TSSOP • E = LQFP-EP

A	Temperature range(°C)	• A= AEC-Q100 Grade 1(-40~125°C) • I= -40~105°C • C= -40~85°C

3.4 Example

This is an example part number: AC7801LFDEA.

4 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate.

Table 4-1 Parameter classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

5 Ratings

5.1 Thermal handling ratings

Table 5-1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, High Temperature Storage Life.
2. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

5.2 Moisture handling ratings

Table 5-2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

5.3 ESD handling ratings

Table 5-3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body discharge mode (other pins except VBAT/LIN)	–4000	4000	V	1
	Electrostatic discharge voltage, human body discharge mode (VBAT, LIN pin)	–8000	8000	V	1
V_{CDM}	Electrostatic discharge voltage, device charging mode (other pins except VBAT/LIN)	–750	750	V	2
I_{LAT}	Latch-up current at ambient temperature of 125°C	–100	100	mA	3

1. Determined according to AEC-Q100-002-D,HUMAN BODY MODEL ELECTROSTATIC DISCHARGE TEST.
2. Determined according to AEC-Q100-011-C1,CHARGED DEVICE MODEL (CDM) ELECTROSTATIC DISCHARGE TEST.
3. Determined according to AEC-Q100-004-D,IC LATCH-UP TEST.
   - Test was performed at 125 °C case temperature (Class II).
   - Supply groups pass 1.5 V_{ccmax}.

- EN PIN@VBAT=24V, other non-power PIN@VBAT=28V.

5.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in the following table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this document.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table 5-4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{BAT}	Battery voltage	-0.3	40	V
V_{CC_O}	High voltage LDO output voltage	-0.3	7	V
V_{DD}	Digital supply voltage	–0.3	6	V
I_{DD}	Maximum current injected into VDD	—	60	mA
V_{IN}	Input voltage except true open drain pins	–0.3	V_{DD} + 0.3 [1]	V
	Input voltage of true open drain pins	–0.3	V_{DD} + 0.3 [1]	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–20	20	mA
EN	LIN PHY enable input port	–0.3	V_{CC_O}+0.3	V
RSTN	LDO reset signal output port	–0.3	V_{CC_O}+0.3	V
LIN	LIN bus input/output port	-40	40	V

[1] Maximum rating of V_{DD} also applies to V_{IN}.

6 General

6.1 Nonswitching electrical specifications

6.1.1 Typical application schematic diagram

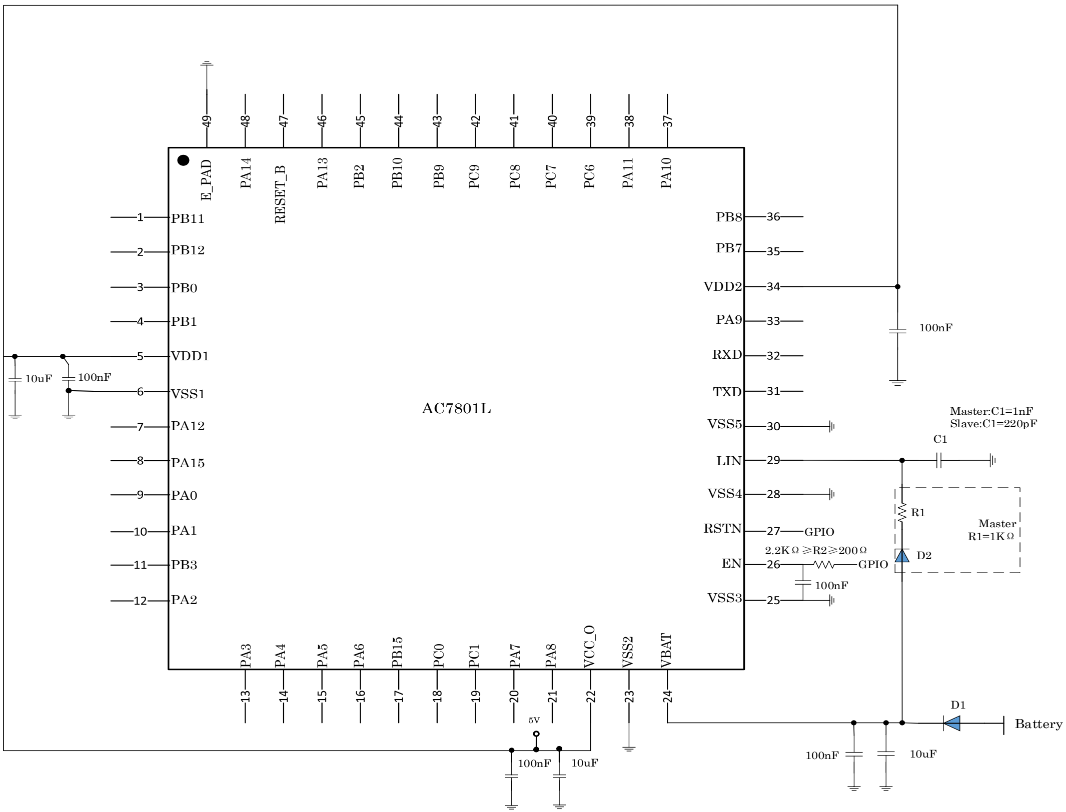

Figure 6-1 Typical application schematic diagram

1. VDD1 and VDD2 can be connected to the same V_{CC_O} on the board and powered by the integrated LDO.
2. All decoupling capacitors must be low ESR ceramic capacitors (X7R type) , the recommended value is 0.1 uF.
3. For improved performance, it is recommended to use 10 uF, 0.1 uF and 1 nF capacitors in parallel.
4. All decoupling capacitors should be placed as close as possible to the corresponding power and ground pins.
5. AC7801L integrates LIN PHY. In multi-point LIN networking applications, the master node needs to use a diode and a 1kΩ resistor in series to pull up the bus. The slave node does not need these two devices and can rely on the internal pull-up of the chip. And usually the master node bus is connected to the ground with a 1nF capacitor, and the slave node bus is connected with a 220pF capacitor to the ground.

6.1.2 DC characteristics

This section includes information about power supply requirements and I/O pin characteristics.

6.1.2.1 MCU DC characteristics

Table 6-1 MCU DC characteristics

Symbol	C	Descriptions			Min.	Typ.	Max.	Unit
—	—	Operating voltage		—	2.7	—	5.5	V
V_{OH}	P	Output high voltage	drive strength	5 V, I_{load} = -5, -10, -15, -20mA	0.85×V_{DD}	—	—	V
	C			3 V, I_{load} = –3.6, -7.2,-10.8,-14.4 mA	0.8×V_{DD}	—	—	V
I_{OHT}	D	Output high current	Max total I_{OH} for all ports	5 V	—	—	30	mA
				3 V	—	—	20	
V_{OL}	P	Output low voltage	drive strength	5 V, I_{load} = 5, 10, 15, 20mA	—	—	0.15×V_{DD}	V
	C			3 V, I_{load} = 3.6, 7.2,10.8,14.4 mA	—	—	0.2×V_{DD}	V
I_{OLT}	D	Output low current	Max total I_{OL} for all ports	5 V	—	—	30	mA
				3 V	—	—	20	
V_{IH}	P	Input high voltage	All digital inputs	4.5≤V_{DD}<5.5 V	0.65×V_{DD}	—	V_{DD} + 0.3	V
				2.7≤V_{DD}<4.5 V	0.70×V_{DD}	—	V_{DD} + 0.3	
V_{IL}	P	Input low voltage	All digital inputs	4.5≤V_{DD}<5.5 V	-0.3	—	0.35×V_{DD}	V
				2.7≤V_{DD}<4.5 V	-0.3	—	0.30×V_{DD}	
V_{hys}	C	Input hysteresis	All digital inputs	—	0.06×V_{DD}	—	—	mV
I_{In}	P	Input leakage current	Per pin (pins in high impedance input mode)	V_{IN} = V_{DD} or V_{SS}	-1	0.1	1	µA
I_{INTOT}	C	Total leakage combined for all port pins	Pins in high impedance input mode	V_{IN} = V_{DD} or V_{SS}	-2	0.1	2	µA

R_{PU}	P	Pullup resistors	All digital inputs, when enabled	—	40	75	190	KΩ
I_{IC}	D	DC injection current	Single pin limit	$V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$	-2	—	2	mA
			Total MCU limit, includes sum of all stressed pins		-5	—	25	
C_{In}	C	Input capacitance, all pins		—	—	5	7	pF
V_{RAM}	C	RAM retention voltage		—	2	—	—	V

Table 6-2 MCU LVD /POR / AVDD Voltage warning specification

Symbol	C	Description	Min.	Typ.	Max.	Unit
V_{POR}	D	POR re-arm voltage [1]	1.6	1.8	2	V
V_{LVDL}	C	Falling low-voltage detect threshold—low range (LVDV= 0)	2.59	2.63	2.68	V
V_{LVDH}	C	Falling low-voltage detect threshold—high range (LVDV=1) [2]	4.22	4.28	4.37	V
V_{HYSLVD}	C	low-voltage detect hysteresis	—	50	—	mV
V_{PVDH}	C	Falling low-voltage warning threshold—high range	4.45	4.6	4.75	V
V_{PVDL}	C	Falling low-voltage warning threshold— low range	2.85	2.95	3.05	V
V_{HYSPVD}	C	Program low-voltage detect hysteresis	—	50	—	mV
V_{BG}	P	Buffered bandgap output [3]	1.18	1.2	1.22	V

[1] Maximum is the highest voltage that POR is guaranteed.

[2] Rising thresholds are falling threshold + hysteresis.

[3] Voltage Factory trimmed at V_{DD} = 5.0 V, Temp = 25 °C.

6.1.2.2 High Voltage LDO and LIN PHY DC Characteristics

Table 6-3 High Voltage LDO and LIN PHY DC Characteristics

Symbol	C	Description	Test Conditions	Min.	Typ.	Max.	Unit
V_{BAT} PIN							
V_{BAT}	P	Battery voltage		5.5	-	28	V
POR(V_{BAT})							
$V_{th(det)pon}$	P	Power-on reset high threshold voltage			4.05	5.25	V
$V_{th(det)poff}$	P	Power-on reset low threshold voltage		3	3.7	4.2	V
$V_{hys(det)pon}$	P	Power-on reset hysteresis voltage		50	350		mV
V_{CC_O} PIN							
V_{CC_O}	P	V_{CC_O} pin voltage		4.9	5	5.1	V
I_{olim}	P	Output current limit	V_{CC_O} =0V to 5.5V	-500	-360	-150	mA
V_{uvd}	P	V_{CC_O} under-voltage detection voltage	$V_{CC\_O\ (nom)}$=5V, Ramp Down	4.3	4.5	4.75	V
V_{uvr}	P	V_{CC_O} under-voltage recovery voltage	$V_{CC\_O\ (nom)}$=5V, Ramp Up	4.4	4.6	4.9	V
Co	D	Output capacitor	Equivalent series resistance <5Ω	1	10		uF
TXD PIN							
$V_{th(SW)}$	P	Switch threshold voltage	V_{CC_O} = 2.97 V ~ 5.5 V	0.3×V_{CC_O}		0.7×V_{CC_O}	V

$V_{hys(i)}$	D	Input hysteresis voltage	V_{CC_O}= 2.97 V ~ 5.5 V	200			mV
R_{pu}	P	Pull-up resistor		5	12	25	kΩ
RXD PIN							
I_{OH}	P	High level output current	Normal mode; V_{RXD}= V_{CC_O} -0.4V; V_{LIN}=V_{BAT}			-0.4	mA
I_{OL}	P	Low level output current	Normal mode; V_{RXD}=0.4V;V_{LIN}=0V	0.4			mA
EN PIN							
$V_{th(sw)}$	P	Switching threshold voltage		0.8		2	V
R_{pd}	P	Pull-down resistor		50	130	400	kΩ
RSTN PIN							
R_{pu}	P	Pull-up resistor	V_{RSTN}=V_{CC_O}-0.4V; V_{CC_O}=2.97V to 5.5V	3	6	12	kΩ
I_{OL}	P	Low level output current	V_{RSTN}=0.4V; V_{CC_O}=2.97V to 5.5V; -40℃<Tvj<195℃	3.2	11	40	mA
V_{OL}	P	low level output voltage	V_{CC_O}=2.5V to 5.5V;-40℃<T_{vj}<195℃	0		0.5	V
V_{OH}	P	High level output voltage	-40℃<T_{vj}<195℃	0.8×V_{CC_O}		V_{CC_O}+0.3	V
LIN PIN							
I_{BUS_LIM}	P	Driver dominant state current limit	V_{TXD}=0V;V_{LIN}=V_{BAT}=18 V	40		150	mA
$I_{BUS\_PAS\_rec}$	P	Receiver recessive input leakage current	V_{TXD}=V_{CC_O} ;V_{LIN}= 18V;V_{BAT}=5.5V			20	μA

$I_{BUS\_PAS\_dom}$	P	Receiver Dominant Input Leakage Current	Normal mode: $V_{TXD}=V_{CC\_O}$; $V_{LIN}=0V$;$V_{BAT}=12V$	-600			μA
$V_{SerDiode1}$	D	Voltage drop of series diode	Pull-up access at Rslave，$I_{SerDiode}=10μA$	0.4		1	V
$I_{BUS\_NO\_GND}$	P	Bus current without ground	$V_{BAT}=18V$; $V_{LIN}=0V$	-750		10	μA
$I_{BUS\_NO\_BAT}$	P	Bus current without power	$V_{BAT}=0V$; $V_{LIN}=18V$			8	μA
V_{BUSdom}	P	Receiver dominant flip threshold voltage	$V_{BAT}=5.5V$ to 18V			$0.4 \times V_{BAT}$	V
V_{BUSrec}	P	Receiver recessive flip threshold voltage	$V_{BAT}=5.5V$ to 18V	$0.6 \times V_{BAT}$			V
V_{BUS_CNT}	P	Receiver center flip threshold voltage	$V_{BAT}=5.5V$ to18V; $V_{BUS\_CNT}=(V_{BUSdom}+V_{BUSrec})/2$	$0.45 \times V_{BAT}$	$0.5 \times V_{BAT}$	$0.55 \times V_{BAT}$	V
V_{HYS}	P	Receiver hysteresis threshold voltage	$V_{BAT}=5.5V$ to 18V; $V_{HYS}=V_{BUSrec}-V_{BUSdom}$			$0.175 \times V_{BAT}$	V
R_{slave}	P	Slave resistance	Resistor between LIN and V_{BAT}, $V_{LIN}=0V$;$V_{BAT}=12V$	20	30	60	kΩ
C_{LIN}	D	LIN pin equivalent capacitance				30	pF
$V_{O(DOM)}$	P	Dominant output voltage	Normal mode; $V_{BAT}=7V$			1.4	V
			Normal mode; $V_{BAT}=18V$			2	V

6.1.3 Supply current characteristics

6.1.3.1 MCU supply current characteristics

Table 6-4 MCU supply current characteristics

Parameter	Symbol	Core/BusFreq	V_{DD} (V)	-40℃	25℃—	85℃	105℃	125℃ [2]	Unit
LFOSC+PLL, all modules clocks enabled	RI_{DD}		5						mA
		48/48 MHz		12.886	12.931	13.188	13.584	13.646	
		48/24 MHz		12.291	12.326	12.583	12.971	13.032	
		24/24 MHz		10.337	10.291	10.512	10.912	10.964	
		12/12 MHz		9.089	8.962	9.163	9.563	9.585	
			3.3						
		48/48 MHz		12.105	12.147	12.434	12.587	12.704	
		48/24 MHz		11.511	11.581	11.792	11.284	12.113	
		24/24 MHz		9.613	9.628	9.805	10	10.12	
		12/12 MHz		8.385	8.341	8.496	8.7	8.799	
LFOSC+PLL, all modules clocks disabled and gated	RI_{DD}		5						mA
		48/48 MHz		9.606	9.63	9.911	9.791	9.882	
		48/24 MHz		9.395	9.49	9.743	9.626	9.724	
		24/24 MHz		7.851	7.857	8.099	7.985	8.079	
		12/12 MHz		6.99	6.974	7.194	7.077	7.148	
			3.3						
		48/48 MHz		8.972	8.976	9.206	9.208	9.302	
		48/24 MHz		8.786	8.84	9.044	9.048	9.163	
		24/24 MHz		7.244	7.238	7.415	7.418	7.517	
		12/12 MHz		6.359	6.369	6.515	6.514	6.606	
XOSC+PLL, all modules clocks enabled	RI_{DD}		5						mA
		48/48 MHz		16.737	17.059	17.532	18.718	18.224	
		48/24 MHz		16.002	16.306	16.796	17.975	17.474	
		24/24 MHz		13.592	13.819	14.268	15.465	14.953	
		12/12 MHz		12.014	12.181	12.624	13.828	13.314	
			3.3						
		48/48 MHz		15.865	16.207	16.649	17.358	17.205	
		48/24 MHz		15.115	15.474	15.907	16.619	16.467	
		24/24 MHz		12.797	13.07	13.49	14.207	14.042	
		12/12 MHz		11.268	11.499	11.905	12.627	12.46	
XOSC+PLL, all modules clocks	RI_{DD}		5						mA
		48/48 MHz		13.008	13.323	13.832	13.836	14.109	

disabled and gated		48/24 MHz		12.825	13.15	13.639	13.646	13.907	
		24/24 MHz		10.862	11.181	11.664	11.645	11.894	
		12/12 MHz		9.805	10.108	10.568	10.559	10.768	
			3.3						
		48/48 MHz		12.315	12.611	13.107	13.214	13.489	
		48/24 MHz		12.127	12.441	12.91	13.013	13.294	
		24/24 MHz		10.193	10.48	10.921	11.027	11.272	
		12/12 MHz		9.137	9.416	9.828	9.927	10.17	
Sleep mode LFOSC+PLL, all modules clocks enabled	RI_{DD}		5						mA
		48/48 MHz		11.787	11.943	12.017	12.109	12.3	
		48/24 MHz		11.183	11.335	11.4	11.49	11.683	
		24/24 MHz		9.689	9.796	9.844	9.923	10.101	
		12/12 MHz		8.636	8.715	8.75	8.825	9.003	
			3.3						
		48/48 MHz		11.185	11.33	11.408	11.493	11.667	
		48/24 MHz		10.588	10.724	10.8	10.887	11.055	
		24/24 MHz		9.107	9.198	9.258	9.333	9.492	
		12/12 MHz		8.059	8.124	8.174	8.244	8.4	
Sleep mode XOSC+PLL, all modules clocks enabled	RI_{DD}		5						mA
		48/48 MHz		15.38	15.828	16.129	16.323	16.69	
		48/24 MHz		14.648	15.086	15.389	15.579	15.939	
		24/24 MHz		12.803	13.199	13.49	13.677	14.021	
		12/12 MHz		11.512	11.875	12.164	12.339	12.677	
			3.3						
		48/48 MHz		14.743	15.144	15.467	15.647	15.986	
		48/24 MHz		14.01	14.398	14.733	14.912	15.251	
		24/24 MHz		12.182	12.537	12.846	13.017	13.343	
		12/12 MHz		10.889	11.223	11.528	11.695	12.019	
Only LFOSC, all modules clocks enabled; HIS_8M	RI_{DD}	8/4 MHz	5	7.104	6.925	7.137	7.432	7.567	
			3.3	6.42	6.39	6.51	6.682	6.81	
Only LFOSC, all modules clocks disabled and gated; HSI_8M	RI_{DD}	8/4 MHz	5	5.173	5.209	5.396	5.281	5.345	
			3.3	4.6	4.619	4.732	4.733	4.828	
Stop mode (RTC/GPIO/I2C/SPI/UART/CAN/LIN can wake up) [3]	SI_{DD}	—	5	3.12	5.94	29.65	55.22	114.11	µA
			3.3	2.71	5.61	28.72	54.42	112.31	

ADC adder to Stop mode	SI_{DD}	—	5	1.93	1.984	2.019	2.05	2.118	mA
			3.3	1.665	1.738	1.754	1.782	1.849	
ADC(wdt enabled) adder to Stop mode(mode2)	SI_{DD}	—	5	106.93	113.63	142.76	167.8	224.95	
			3.3	99.66	106.79	136.32	160.86	217.73	
ACMP adder to Stop mode	SI_{DD}	—	5	18.35	21.51	45.17	70.87	129.59	µA
			3.3	14.94	17.91	40.82	66.96	124.97	
LVD adder to Stop mode	SI_{DD}	—	5	37.97	42.74	67.82	93.89	153.46	µA
			3.3	34.65	39.55	64.49	90.8	149.72	
Standby mode(RTC on, RTC/NMI can wake up) [3]	SI_{DD}	—	5	1.95	2.31	7.12	12.54	27	µA
			3.3	1.47	2	6.59	11.88	25.78	

[1] Data in Typical column was characterized at 3.3/5.0 V, 25 °C or is typical recommended value.

[2] Data in Typical column was characterized at 3.3/5.0 V, 125 °C or is typical recommended value.

[3] RTC adder cause <1 µA I_{DD} increase typically, RTC clock source is 32 kHz LPO clock.

6.1.3.2 High voltage LDO+LIN PHY supply current characteristics

Table 6-5 High voltage LDO+LIN PHY supply current

Parameter	C	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
V_{BAT} pin current	P	I_{BAT}	Standby：V_{LIN}=V_{BAT}		22	52	µA
			Sleep：V_{LIN}=V_{BAT}		14	28	µA
			Normal（rec）：V_{LIN}=V_{BAT} V_{RXD}=VCC		135	850	µA
			Normal（dom）：V_{BAT}=12V V_{RXD}=0		1.5	4	mA

6.2 Switching specifications

6.2.1 Control timing

Table 6-6 Control timing

Num	C	Rating	Symbol	Min.	Typ. [1]	Max.	Unit
1	D	System and core clock (t_{sys} = 1/f_{Sys})	f_{Sys}	DC	—	48	MHz
2	P	Bus frequency (t_{cyc} = 1/f_{Bus})	f_{Bus}	DC	—	48 [2]	MHz
3	P	Internal low power oscillator frequency	f_{LPO}		32		KHz
4	D	External reset pulse width [3]	t_{extrst}	1.5 × t_{32k}	—	—	ns
5	D	IRQ pulse width — Run mode [4]	t_{ILIH}/ t_{IHIL}	1.5 × t_{sys}	—	—	ns

	D		Stop mode [4]	t_{ILIH}/ t_{IHIL}	$1.5 \times t_{32k}$	—	—	ns
6	D	Port rise and fall time - Normal drive strength(load = 50 pF) [5]	—	t_{Rise}	—	10.2	—	ns
	D			t_{Fall}	—	9.5	—	ns
	D	Port rise and fall time - high drive strength(load = 50 pF) [5]	—	t_{Rise}	—	5.4	—	ns
	D			t_{Fall}	—	4.6	—	ns

[1] Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

[2] The maximum operating frequency of AC7801L series, please refer to the product selection table.

[3] This is the shortest pulse that is guaranteed to be recognized as a RESET_B pin request.

[4] This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized.

[5] Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature ranges -40 °C to 125 °C.

6.2.2 PWM module timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the PWM clock.

Table 6-7 PWM input timing

C	Function	Symbol	Min.	Max.	Unit
D	Timer clock frequency	f_{PWM}	—	48M	Hz
D	Input capture pulse width	t_{ICPW}	1.5	—	t_{PWM} [1]

[1] $t_{PWM} = 1/ f_{PWM}$

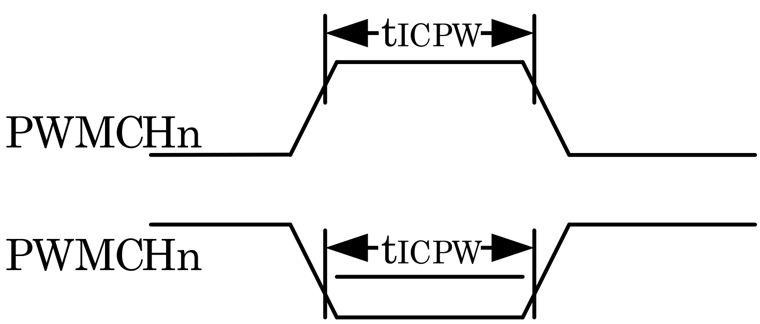

Figure 6-2 Timer input capture pulse

6.3 Thermal specifications

6.3.1 Thermal characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user- determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 6-8 Thermal characteristics

Board type	Symbol	Description	48 LQFP-EP	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	74.9	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	44.3	°C/W	1, 3
-	$R_{\theta JB}$	Thermal resistance, junction to board	26.7	°C/W	4
-	$R_{\theta JC}$	Thermal resistance, junction to case	33.0	°C/W	5
Single-layer (1s)	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center(natural convection)	6.5	°C/W	6
Four-layer (2s2p)	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center(natural convection)	5.2	°C/W	6
Single-layer (1s)	Ψ_{JB}	Thermal characterization parameter, junction to package bottom outside center(natural convection)	35.4	°C/W	7
Four-layer (2s2p)	Ψ_{JB}	Thermal characterization parameter, junction to package bottom outside center(natural convection)	27.9	°C/W	7

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
3. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

The average chip-junction temperature (T_J) in °C can be obtained from:

$T_J = T_A + (P_D \times \theta_{JA})$ Where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts - chip internal power

$P_{I/O}$ = Power dissipation on input and output pins - user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$P_D = K \div (T_J + 273\ °C)$

Solving the equations above for K gives: $K = P_D \times (T_A + 273\ °C) + \theta_{JA} \times (PD)^2$

where K is a constant pertaining to the particular part. K can be determined by measuring

P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving the above equations iteratively for any value of T_A.

7 Peripheral operating requirements and behaviors

7.1 Core modules

7.1.1 SWD electricals

Table 7-1 SWD full voltage range electrical

Symbol	Description	Min.	Max.	Unit
—	Operating voltage	2.7	5.5	V
J1	SWD_CLK frequency of operation • Serial wire debug	0	20	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	5	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	5	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	41	ns

7.2 External oscillator (OSC) and ICS characteristics

7.2.1 External oscillator(OSC) characteristics

Table 7-2 OSC specifications (temperature range = -40 to 125 °C ambient)

Num	C	Characteristic	Symbol	Min.	Typ.	Max.	Unit
1	C	Crystal frequency	f_{hi}	4	—	30	MHz
2	D	Load capacitors	C_{L1}, C_{L2}	See Note [1]			
3	D	Series resistor	RS	—	0	—	KΩ
4	C	Crystal start-up time	t_{CST}	—	3	—	ms

[1] For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors designed for high-frequency applications, and selected to match the requirements of the crystal. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

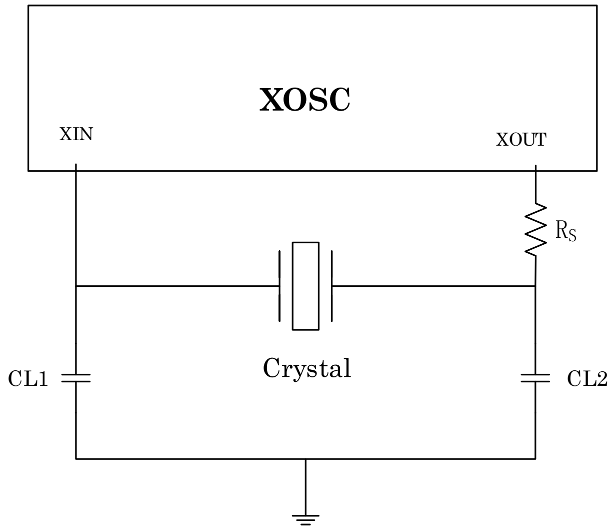

Figure 7-1 Typical crystal or resonator circuit

7.2.2 Internal RC characteristics

Table 7-3 OSC and ICS specifications (temperature range = -40 to 125 °C ambient)

Num	C	Characteristic		Symbol	Min.	Typ.	Max.	Unit
1	P	LFOSC output frequency range	Over temperature range from -40 °C to 125°C	f_{lfosc}	7.88	8	8.12	MHz
2	P	LPOSC Internal reference clock frequency, factory trimmed	T = 25 °C, V_{DD} = 5 V	f_{int_ft}	—	32	—	kHz
3	P	LPOSC Factory trimmed internal oscillator accuracy	T = 25 °C, V_{DD} = 5 V	Δf_{int_ft}	-4	—	4	%
4	P	LPOSC Deviation of IRC over temperature when trimmed at T = 25 °C, V_{DD} = 2.7-5.5 V	Over temperature range from -40 °C to 125°C	Δf_{int_t}	-20	—	15	%

7.2.3 PLL characteristics

Table 7-4 PLL characteristics

No.	Symbol	Parameter	Min.	Typ.	Max.	Unit
1	f_{PLL_IN}	PLL input clock frequency	4	—	30	MHz

No.	Symbol	Parameter	Min.	Typ.	Max.	Unit
2	f_{PLL_REF}	PFD input clock frequency	—	—	8	MHz
3	f_{PLL_OUT}	PLL output clock frequency	9	—	750	MHz
4	f_{VCO_OUT}	VCO output frequency	500	—	1500	MHz
Operating condition: junction temperature -40~125°C f_{PLL_OUT} is f_{VCO_OUT} /Postdiv, Postdiv can be 2,4,6,…,60,62 f_{PLL_REF} is f_{PLL_IN} /Prediv, Prediv can be 1,2,4.						

7.3 Embedded Flash specifications

This section provides details about program/erase/read parameters and reliability features for the Flash memory.

Table 7-5 Flash characteristics

C	Characteristic	Symbol	Min.	Typ.	Max.	Unit
D	Supply voltage for program/erase at temperature from - 40°C to 125 °C	$V_{prog/erase}$	2.7	—	5.5	V
D	Supply voltage for read operation at temperature from -	V_{Read}	2.7	—	5.5	V
D	Flash Bus frequency	f_{SYS}	8		48	MHz
D	Mass Erase (all Main Block pages)	t_{MER}	—	114.6	—	ms
D	Page Erase (one page)	t_{PER}	—	114.6	—	ms
D	Mass Erase Verify	t_{MERV}	65600	—	131200	t_{cyc} [1]
D	Page Erase Verify	t_{PERV}	535	—	1070	t_{cyc} [1]
D	Program Flash (1 word)	t_{PRG1}	—	66.5	—	us
D	Program Flash (n word, n>1)	t_{PRGn}	—	66.5+14.6× (n-1)	—	us
C	Flash Program/erase endurance at temperature from - 40°C to 125 °C	n_{EDR}	10 k	—	—	cycles
C	Data retention at an average junction temperature of TJavg = 85°C after up to 10,000 program/erase cycles	t_{RET}	10	—	—	years

[1] t_{cyc} = 1/ f_{SYS}.

7.4 Analog

7.4.1 ADC and Tsensor characteristics

Table 7-6 12 bit ADC and Tsensor Operating Conditions and Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{AVDD}	Supply Voltage	Absolute	2.7	—	5.5	V
V_{IN}	Input Voltage Range	—	0	—	V_{AVDD}	V
R_{IN}	Source impedance	—	—	1.0 [1]	—	KΩ
C_{ADC}	Internal Sampling Capacitor	—	—	2.3	—	pF
R_{ADC}	Sampling switch resistance	—	—	2.6	—	KΩ
f_{ADC}	ADC Clock Frequency	—	—	—	24	MHz
f_{sample}	Sampling Time	—	280	—	—	ns
frate	Conversion Rate	f_{ADC}=24 MHz	—	—	1	MHz
INL	Integral Non-Linearity	—	—	1.5	—	LSB [2]
DNL	Differential Non-Linearity	—	—	1.5	—	LSB [2]
CH	External Channels	—	—	—	12	-—

[1] Value based on 291 ns sampling time condition

[2] LSB = V_{AVDD} /2^{12}

Table 7-7 12 bit ADC and Tsensor Operating Conditions and Characteristics(continue)

Characteristic	Conditions	C	Symbol	Min.	Typ.	Max.	Unit
Temp sensor slope	-40 °C~125 °C	D	Slope	—	1.629	—	mV/°C
Temp sensor voltage	25 °C	D	V_{TEMP25}	—	0.72	—	V

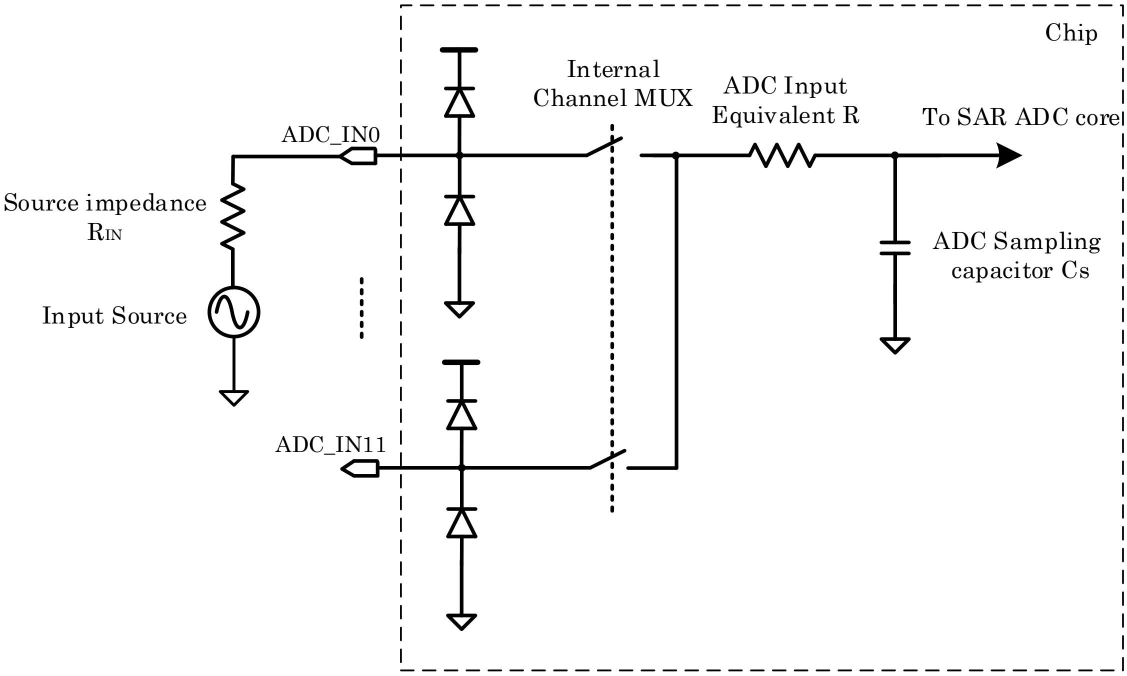

Figure 7-2 ADC input equivalent diagram

7.4.2 Analog comparator (ACMP) electricals

Table 7-8 Comparator electrical specifications

C	Characteristic	Symbol	Min.	Typ.	Max.	Unit
D	Supply voltage	V_{AVDD}	2.5	—	5.5	V
T	Supply current (Operation mode)	I_{DDA}	—	—	20	µA
D	Analog input voltage	V_{AIN}	V_{SS} - 0.3	—	V_{AVDD}	V
D	Analog input offset voltage	V_{AIO}	—	—	40	mV
D	Analog comparator hysteresis (HYST=0)	V_H	—	20	—	mV
D	Analog comparator hysteresis (HYST=1)	V_H	—	40	—	mV
T	Supply current (Off mode)	I_{DDAOFF}	—		100	nA
C	Propagation Delay	t_D	—	0.4	1	µs

7.5 Communication interfaces

7.5.1 SPI specifications

The serial peripheral interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's reference manual for information about the modified transfer formats used for communicating with slower peripheral devices. All timing is shown with respect to 20% V_{DD} and 80% V_{DD}, unless noted, and 25 pF load on all SPI pins. All timing assumes slew rate control is disabled and high-drive strength is enabled for SPI output pins.

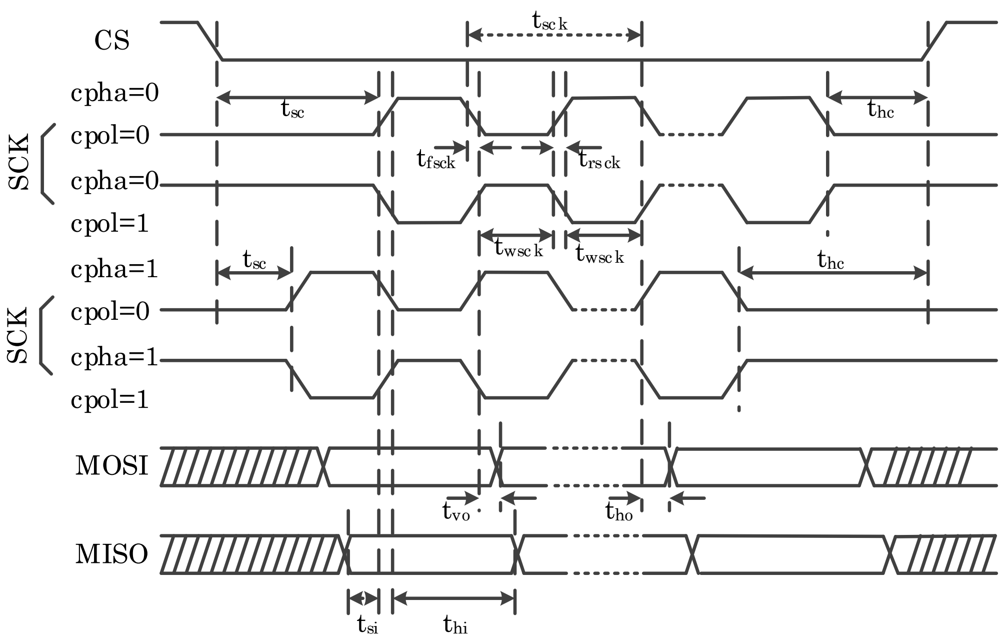

Figure 7-3 SPI timing diagram – master

Table 7-9 SPI characteristics – master

Symbol	Description	Min.	Max.	Unit	Comment
f_{op}	Frequency of operation	$f_{bus}/512$	$f_{bus}/2$	Hz	f_{bus} is bus clock
t_{sc}	CS setup time	$1\times t_{bus}$	$256\times t_{bus}$	ns	Negative edge of CS to first SCK edge
t_{hc}	CS hold time	$1\times t_{bus}$	$256\times t_{bus}$	ns	Last SCK edge to positive edge of CS
t_{wsck}	SCK high or low level time	$1\times t_{bus}$	$256\times t_{bus}$	ns	No considering t_{rsck} and t_{fsck}
t_{si}	Data input setup time	16	—	ns	—
t_{hi}	Data input hold time	16	—	ns	—
t_{vo}	Data output valid time	—	7	ns	—
t_{ho}	Data output hold time	1	—	ns	—

Symbol	Description	Min.	Max.	Unit	Comment
t_{rsck}	Clock output rise time	4.5	15.4	ns	—
t_{fsck}	Clock output fall time	5.1	16.2	ns	—

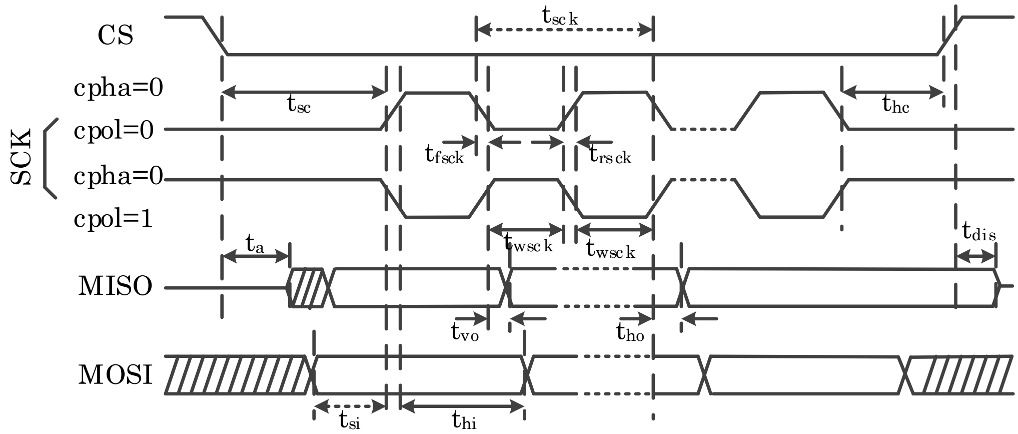

Figure 7-4 SPI timing diagram – slave(cpha=0)

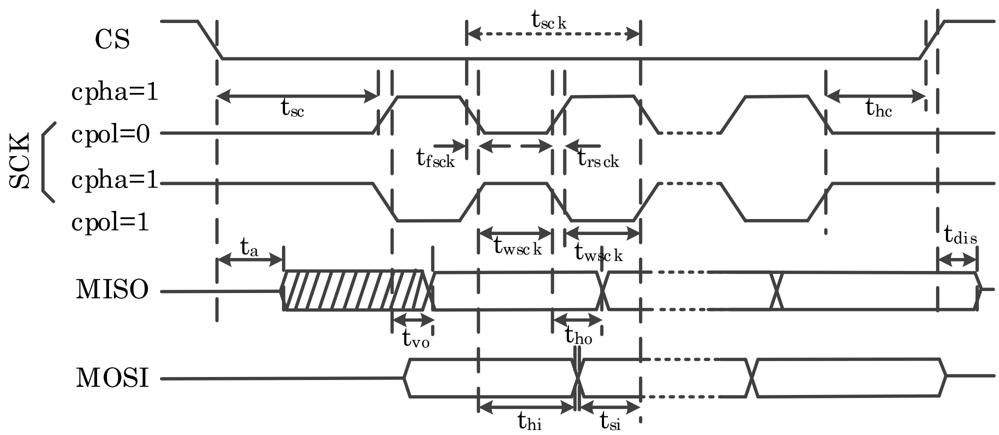

Figure 7-5 SPI timing diagram – slave(cpha=1)

Table 7-10 SPI characteristics - slave

Symbol	Description	Min.	Max.	Unit	Comment
f_{op}	Frequency of operation	—	12 M	Hz	
t_{sc}	CS setup time	$2\times t_{bus}$	—	ns	Negative edge of CS to first SCK edge
t_{hc}	CS hold time	$2\times t_{bus}$	—	ns	Last SCK edge to positive edge of CS
t_a	slave access time	—	t_{bus}	ns	Data from “Z” to effective
t_{dis}	slave MISO disable time	—	t_{bus}	ns	Data from effective to “Z”
t_{wsck}	SCK high or low level time	30%	70%	—	—

Symbol	Description	Min.	Max.	Unit	Comment
t_{si}	Data input setup time	12	—	ns	—
t_{hi}	Data input hold time	28	—	ns	—
t_{vo}	Data output valid time	—	36 [1] 29 [2]	ns	—
t_{ho}	Data output hold time	14	-	ns	—
t_{rsck}	Clock input rise time	1.4	5.4	ns	—
t_{fsck}	Clock input fall time	1.4	6.4	ns	—

[1] GPIO setting 00

[2] GPIO setting 10

7.5.2 CAN specifications

Table 7-11 CAN wake-up pulse characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
CAN wakeup dominant pulse filtered	t_{WUP}	—	—	0.9	µs
CAN wakeup dominant pulse pass	t_{WUP}	4.7	—	—	µs

7.5.3 UART specifications

Basic function of Universal Asynchronous Receiver/Transmitter (UART) is to transmit and receive the serial data bit by bit. In order to support transmitting break field, sync field and data, additional Soft Local Interconnect Network(LIN) is included in the AC7801L chips. The main parameters of UART is introduced as below:

1. Up to 3 UART function channels and two of which support soft LIN functions (the uart function and LIN function of the same UART cannot be used at the same time).
2. UART can transmit or receive data with the range of baud rate from 600 bps to 3 Mbps, and the tolerance of real baud rate with ideal baud rate is less than 1%.
3. The minimum GPIO pin interrupt pulse width is 333 ns. Because of that these pins do not have a passive filter on the inputs, this is the shortest pulse width that is guaranteed to be recognized.
4. The maximum baud rate supported in soft LIN function is 20 kbps.
5. Auto baud rate detection is selectable open or not in soft LIN function. The tolerance of received baud rate is from -20%(+/-2%)to +23% (+/-2%) , in this case.

7.5.4 I2C specifications

Table 7-12 Characteristics of the I2C bus lines for different mode

Symbol	Parameter	Standard-mode		Fast-mode		Fast-mode Plus		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCL}	SCL clock frequency	0	100	0	400	0	1000	kHz
$t_{HD;STA}$	hold time (repeated) START condition	4	—	0.6	—	0.26	—	µs
t_{LOW}	LOW period of the SCL clock	4.7	—	1.3	—	0.5	—	µs
t_{HIGH}	HIGH period of the SCL clock	4	—	0.6	—	0.26	—	µs
$t_{SU;STA}$	set-up time for a repeated START condition	4.7	—	0.6	—	0.26	—	µs
$t_{HD;DAT}$	data hold time	0	—	0	—	0	—	µs
$t_{SU;DAT}$	data set-up time	250	—	100	—	50	—	ns
t_r	rise time of both SDA and SCL signals	—	1000	20	300	—	120	ns
t_f	fall time of both SDA and SCL signals	—	300	20 × (V_{DD} / 5.5 V)	300	20 × (V_{DD} / 5.5 V)	120	ns
$t_{SU;STO}$	set-up time for STOP condition	4	—	0.6	—	0.26	—	µs
t_{BUF}	bus free time between a STOP and START condition	4.7	—	1.3	—	0.5	—	µs
C_b	capacitive load for each bus line	—	400	—	400	—	550	pF
$t_{VD;DAT}$	data valid time	—	3.45	—	0.9	—	0.45	µs
$t_{VD;ACK}$	data valid acknowledge time	—	3.45	-	0.9	-	0.45	µs

V_{nL}	noise margin at the LOW level	$0.1V_{DD}$	—	$0.1V_{DD}$	—	$0.1V_{DD}$	—	V
V_{nH}	noise margin at the HIGH level	$0.2V_{DD}$	—	$0.2V_{DD}$	—	$0.2V_{DD}$	—	V

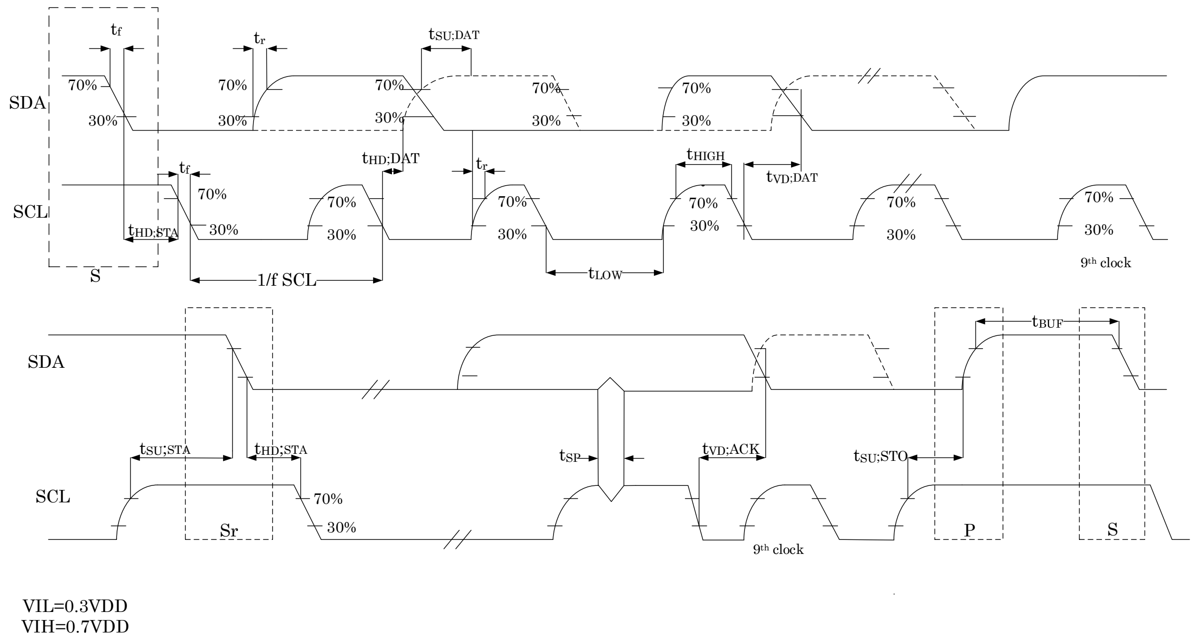

Figure 7-6 Definition of timing for F/S-mode devices on the I2C-bus

7.6 High voltage LDO+LIN PHY

Integrated high voltage LDO and LIN PHY. LDO supports a wide voltage input range of 5.5V to 28V and supplies power to MCU or other peripheral devices through the V_{CC_O} pin. The LDO output voltage is fixed at 5V and can provide an output current capability of 70mA. In applications, it should be appropriately derated according to the input VBAT voltage and ambient temperature. LIN PHY is compatible with the "LIN 2.x/ISO 17987-4:2016/SAE J2602" standard and supports 12V applications.

7.6.1 Short circuit protection

The chip has V_{CC_O} output voltage short-circuit protection and LIN bus short-circuit protection. When the V_{CC_O} output is short-circuited to GND, the internal circuit limits the maximum current to within I_{Olim} through current limiting, thereby preventing the chip from burning due to excessive power consumption; when the LIN bus voltage is short-circuited to the V_{BAT} power supply and the chip is in a dominant state, the transmitter internally limits the maximum current to I_{BUS_LIM} through current limiting, thereby preventing the chip from burning due to excessive power consumption.

7.6.2 V_{CC_O} under voltage protection

The LDO output voltage is continuously monitored and ultimately reflected on the system reset signal RSTN. When V_{CC_O}<V_{uvd} and the duration exceeds $t_{det(uv)(VCC\_O)}$, the RSTN output is pulled low; when V_{CC_O}>V_{uvr} and the duration exceeds t_{rst}, the RSTN output is pulled high.

7.6.3 Over temperature protection

The chip has over-temperature protection function. In shutdown mode, normal mode and standby mode, when the junction temperature exceeds the shutdown junction temperature $T_{th(act)otp}$, the chip will enter shutdown mode, LDO will turn off, and RSTN becomes low level; when the junction temperature drops below $T_{th(rel)otp}$, the chip re-enters standby mode and LDO turn on normally. In sleep mode, the LDO and transmitter are already in shutdown state, even if the over-temperature protection is triggered, the chip remains in sleep mode.

Table 7-13 Over temperature threshold

C	Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
T	Shut-down junction temperature	$T_{th(act)otp}$	--	165	180	195	℃
T	Recovery junction temperature	$T_{th(rel)otp}$	--	126	138	150	℃

7.6.4 Dominant timeout

The built-in TXD(PC2) dominant timeout timer circuitry prevents the bus line from being driven to a permanently dominant state (blocking all Telecommunication). The timer is triggered by the falling edge of the TXD(PC2) signal. If TXD(PC2) remains low for longer than the internal timer time ($t_{to(dom)TXD}$), the transmitter will be disabled and drive the bus into a recessive state. The timer is reset by the rising edge of the TXD(PC2) signal.

7.6.5 Remote wake up

When the LIN pin is pulled low to a low level through a falling edge, a rising edge appears at the next moment, and the low-level maintenance time between the rising edge and the falling edge at the previous moment is greater than $t_{wake(dom)LIN}$, then this process is considered a valid remote wakeup (shown in Figure 7-7). When a valid remote wake-up event occurs, the chip enters standby mode, and RXD (PC3) is a continuous low level.

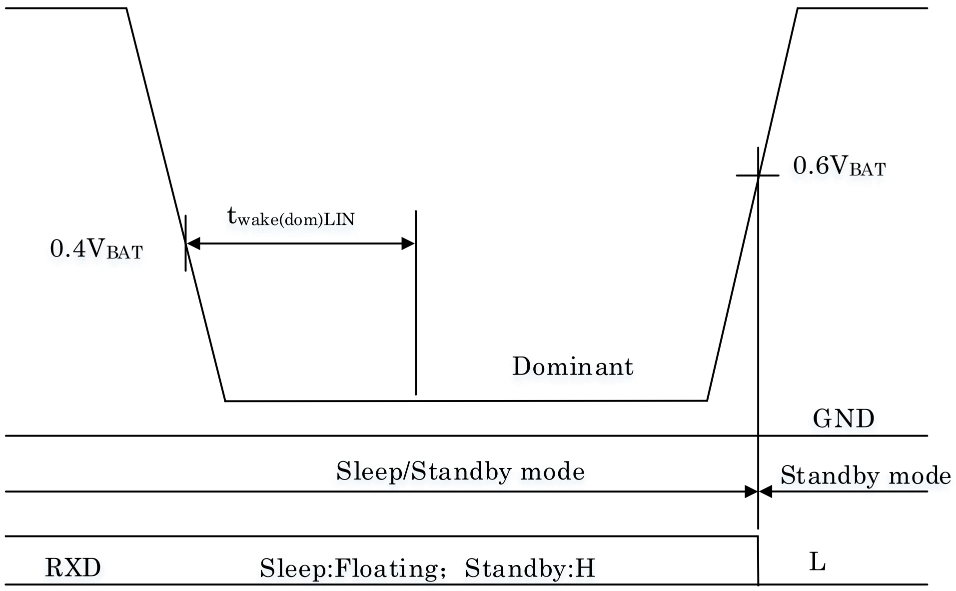

Figure 7-7 Remote wake-up behavior

7.6.6 Timing characteristics

Table 7-14 Timing characteristics

C	Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
P	Receiver propagation delay	$t_{P(RX)}$	rise and fall，C_{RXD}=5pF	--	--	6	µs
P	Receiver Propagation Delay Symmetry	$t_{P(RX)sym}$	C_{RXD}=5pF	-2	--	2	µs
P	LIN dominant wake-up time	$t_{wake(dom)LIN}$	Sleep mode，Figure 7-7	30	80	150	µs
P	TXD dominant time-out	$t_{to(dom)TXD}$	V_{TXD}=0V	6	13	20	ms
P	Mode select time	t_{msel}		3	11.5	20	µs

P	Under-voltage detection time on V_{CC_O}	$t_{det(uv)(VCC\_O)}$	C_{RSTN}=20pF	1	8	15	μs
P	Reset time	t_{rst}		2		8	ms

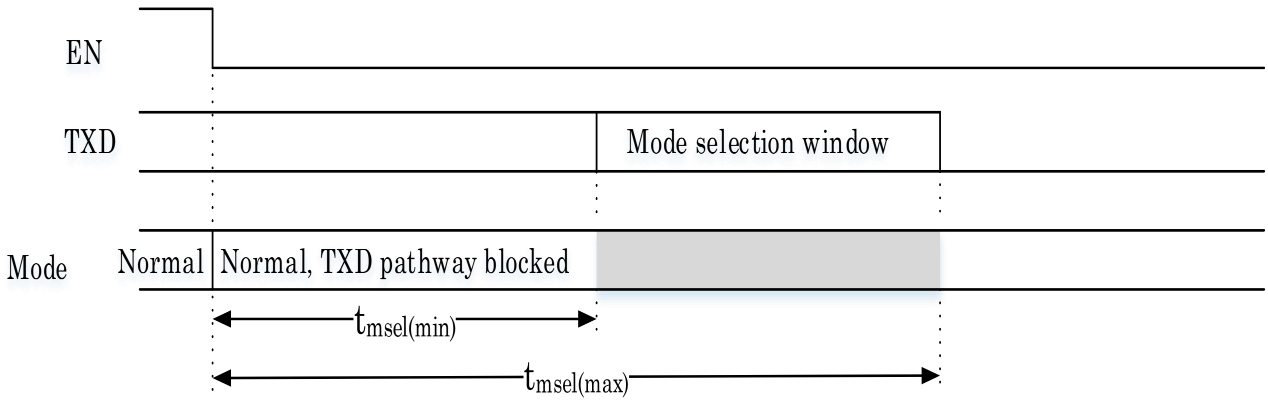

Figure 7-8 Transition from Normal to Sleep/Standby mode

7.6.7 Dynamic characteristics

Table 7-15 Duty cycle

C	Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
P	Duty cycle 1	$\delta 1$[1,2]	$V_{th(rec)(max)}$=0.744xV_{BAT}; $V_{th(dom)(max)}$=0.581xV_{BAT}; t_{bit}=50μs; V_{BAT}=7V~18V, Figure 7-9	0.396	--	--	--
			$V_{th(rec)(max)}$=0.76xV_{BAT}; $V_{th(dom)(max)}$=0.593xV_{BAT}; t_{bit}=50μs; V_{BAT}=5.5V~7V, Figure 7-9	0.396			
P	Duty cycle 2	$\delta 2$[2,3]	$V_{th(rec)(min)}$=0.422xV_{BAT}; $V_{th(dom)(min)}$=0.284xV_{BAT}; t_{bit}=50μs; V_{BAT}=7.6V~18V, Figure 7-9	--	--	0.581	--

C	Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
			$V_{th(rec)(min)}$=0.41xV_{BAT}; $V_{th(dom)(min)}$=0.275xV_{BAT}; t_{bit}=50μs; V_{BAT}=6.1V~7.6V，Figure 7-9	--	--	0.581	--
P	Duty cycle 3	δ3[1,2]	$V_{th(rec)(max)}$=0.778xV_{BAT}; $V_{th(dom)(max)}$=0.616xV_{BAT}; t_{bit}=96μs; V_{BAT}=7V~18V，Figure 7-9	0.417	--	--	--
			$V_{th(rec)(max)}$=0.797xV_{BAT}; $V_{th(dom)(max)}$=0.630xV_{BAT}; t_{bit}=96μs; V_{BAT}=5.5V~7V，Figure 7-9	0.417	--	--	--
P	Duty cycle 4	δ4[2,3]	$V_{th(rec)(min)}$=0.389xV_{BAT}; $V_{th(dom)(min)}$=0.251xV_{BAT}; t_{bit}=96μs; V_{BAT}=7.6V~18V，Figure 7-9	--	--	0.59	--
			$V_{th(rec)(min)}$=0.378xV_{BAT}; $V_{th(dom)(min)}$=0.242xV_{BAT}; t_{bit}=96μs; V_{BAT}=6.1V~7.6V，Figure 7-9	--	--	0.59	--

注：

1.δ1, δ3= $\frac{t_{\text{bus(rec)(min)}}}{2\times t_{bit}}$

2.Bus load conditions：(1) C_{BUS}=1nF,R_{BUS}=1kΩ；(2) C_{BUS}=6.8nF,R_{BUS}=660Ω；(3) C_{BUS}=10nF, R_{BUS}=500Ω

3.δ2, δ4= $\frac{t_{\text{bus(rec)(max)}}}{2\times t_{bit}}$

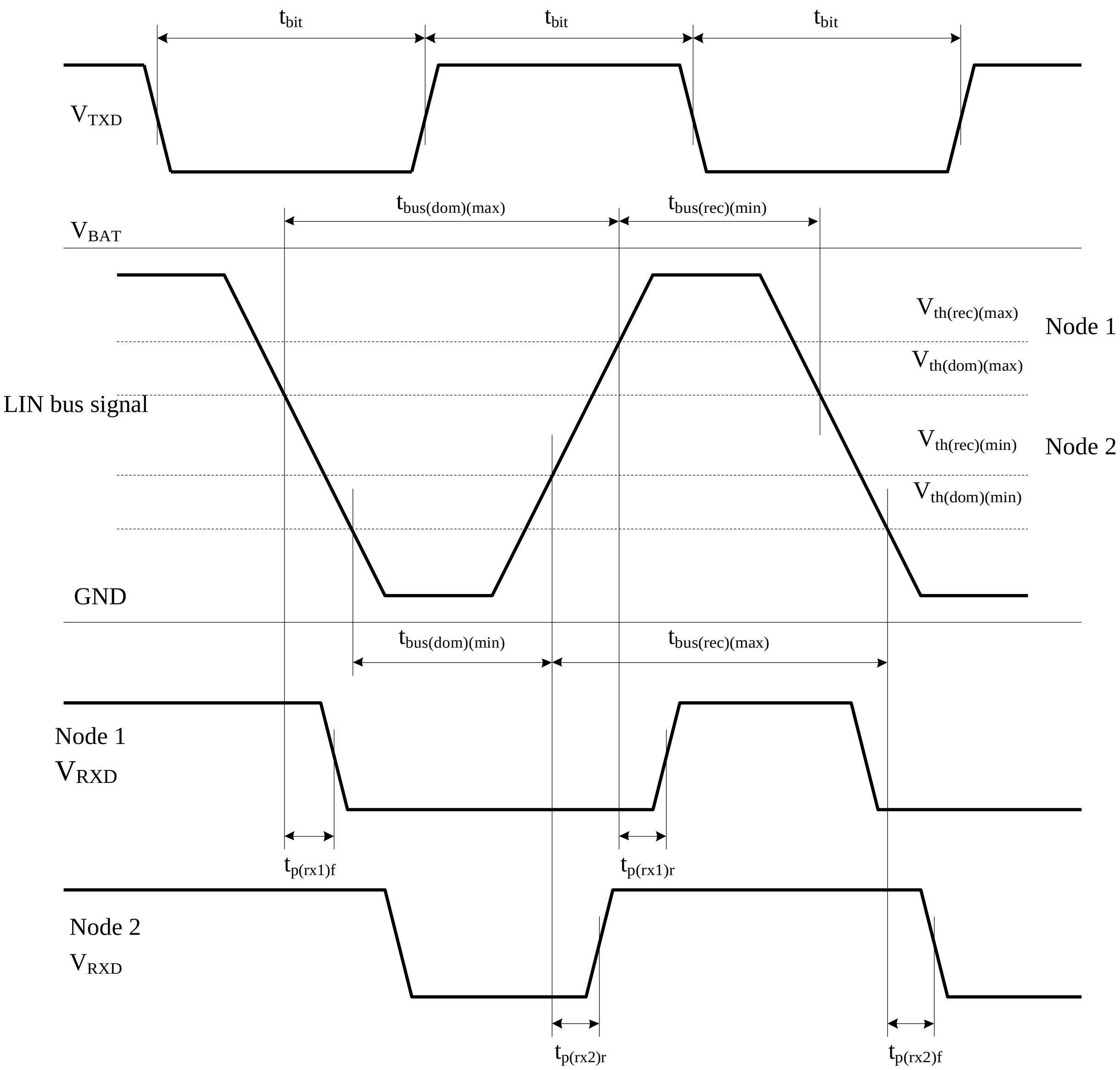

Figure 7-9 LIN transceiver timing diagram

7.6.8 Operating mode

There are four main working modes, namely sleep mode, standby mode, normal mode and shutdown mode[1].

- **Shutdown mode:** When the V_{BAT} voltage is less than the power-on detection voltage threshold $V_{th(det)poff}$ or over-temperature protection occurs, the chip will be in shutdown mode, the voltage regulator and LIN transceiver are turned off, RSTN = 0.。
- **Standby mode:** When the chip is in sleep mode and detects a remote wake-up event, or in normal mode it detects EN=L and TXD(PC2)=H, and RSTN=H (V_{CC_O} voltage is output normally), or in shutdown mode. When V_{BAT} is not under-voltage and the chip is not overheated, the chip enters standby mode. While in standby mode, the transmitter is turned off and RXD(PC3) represents a wake-up event.
- **Normal mode:** When the chip detects EN=H and RSTN=H in standby mode, or detects EN=H in sleep mode, the chip enters normal mode. When in normal mode, the LIN transceiver is turned on, a high level on the bus represents recessive, and a low level represents dominant. The receiver detects the data flow on the LIN bus input pin and outputs it to RXD (PC3).
- **Sleep mode:** When the chip is in normal mode and detects EN going from high to low and TXD(PC2)=0 and RSTN=1, the chip enters sleep mode. When in sleep mode, the LDO function is turned off, the LIN transceiver is turned off, and RSTN is pulled low.

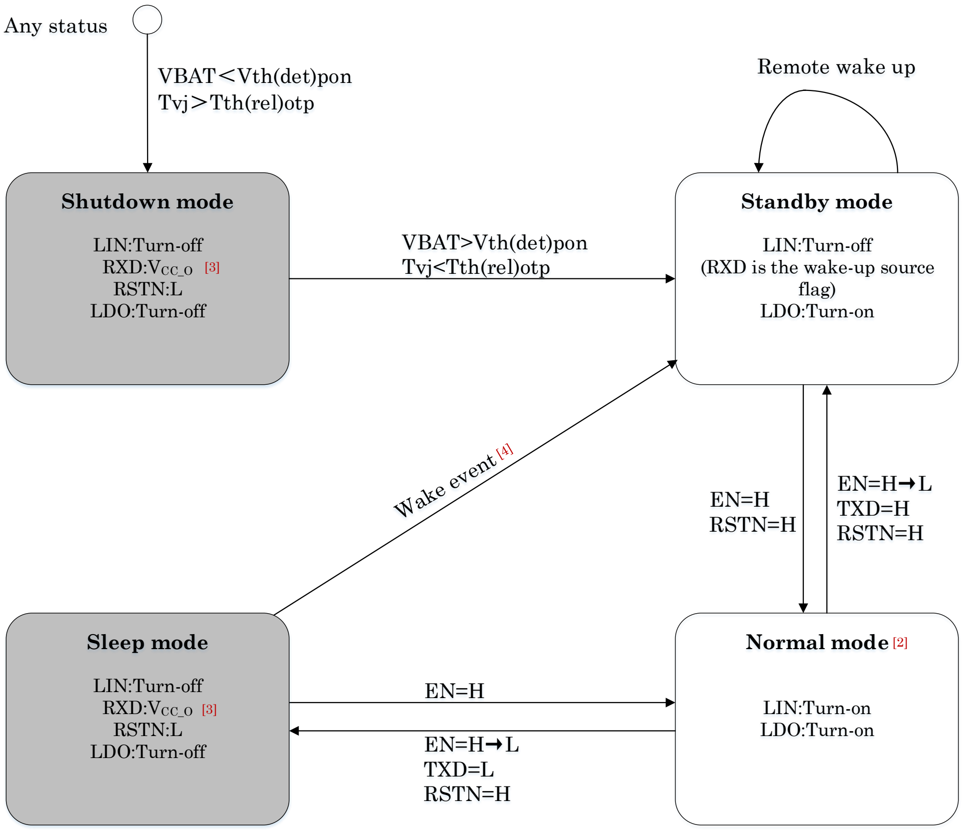

Figure 7-10 State diagram[1]

[1] Only the operation mode and wake-up method of LIN PHY. For detailed operation mode and wake-up method of AC7801L, please refer to《AC7801L Reference Manual》.

[2] In Normal mode, the LIN transmitter is enabled, but if EN and/or RSTN become LOW, the LIN transmitter will be disabled. Remote wake-up function will be activated.

[3] Until V_{CC_O} drops below 2 V, else floating.

[4] If a wake-up event and a go-to-sleep event occur simultaneously, the device will turn directly to Standby mode without initiating a reset.

8 Dimensions

8.1 LQFP48-EP package information

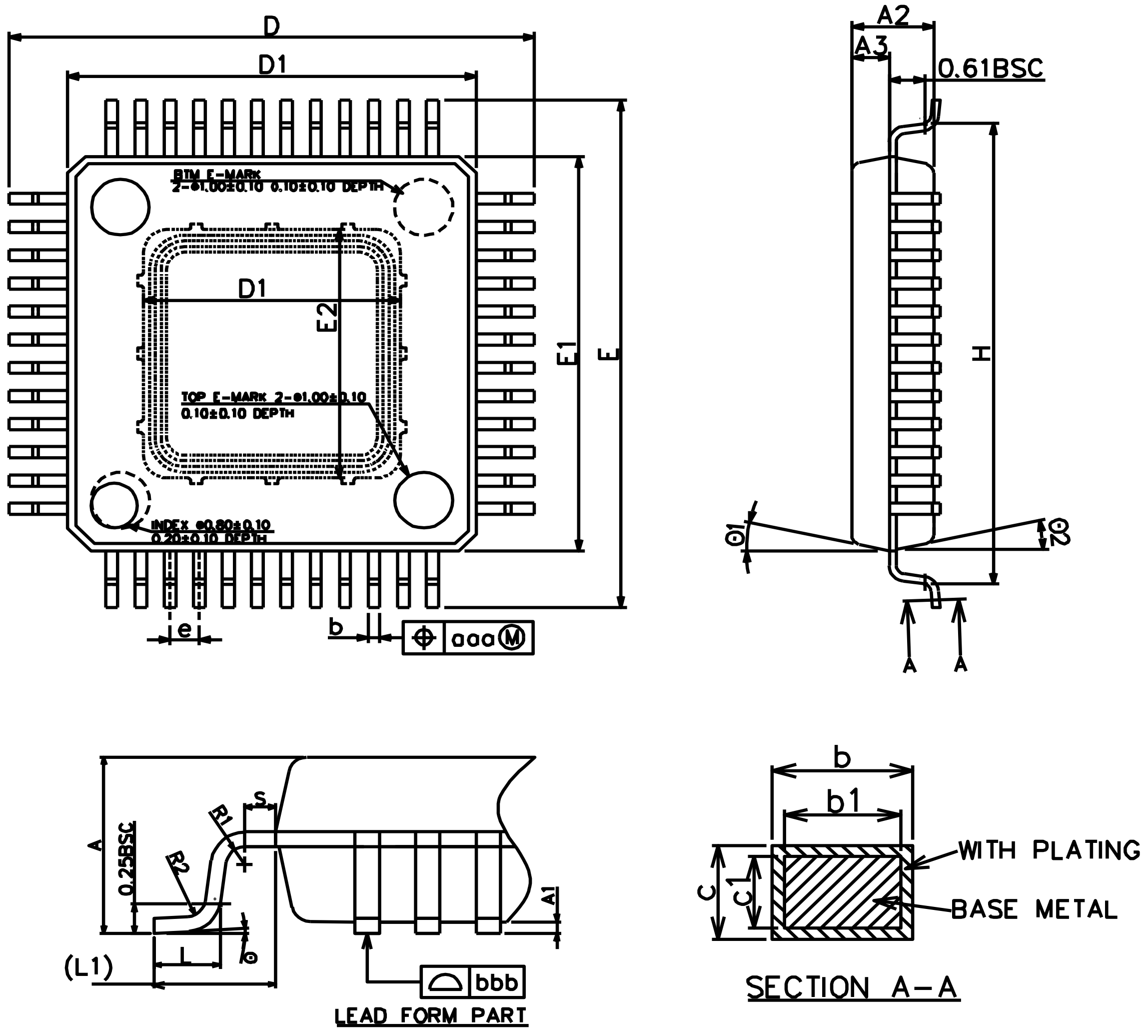

Figure 8-1 LQFP48-EP , 7 x 7 mm low-profile quad flat package outline [1]

[1] Drawing is not to scale.

Table 8-1 LQFP48-EP, 7 x 7 mm low-profile quad flat package mechanical data [1]

<table>
<tr><th colspan="2">ITEM</th><th>SYMBOL</th><th>Min.</th><th>NOM.</th><th>Max.</th></tr>
<tr><td colspan="2">Total height</td><td>A</td><td>—</td><td>—</td><td>1.60</td></tr>
<tr><td colspan="2">Stand off</td><td>A1</td><td>0.05</td><td>—</td><td>0.15</td></tr>
<tr><td colspan="2">Mold thickness</td><td>A2</td><td>1.35</td><td>1.40</td><td>1.45</td></tr>
<tr><td colspan="2">Leadframe to mold height</td><td>A3</td><td>0.59</td><td>0.64</td><td>0.69</td></tr>
<tr><td colspan="2">Lead width</td><td>b</td><td>0.18</td><td>—</td><td>0.27</td></tr>
<tr><td colspan="2">Lead width without plating</td><td>b1</td><td>0.17</td><td>0.20</td><td>0.23</td></tr>
<tr><td colspan="2">Leadframe thickness</td><td>c</td><td>0.13</td><td>—</td><td>0.18</td></tr>
<tr><td colspan="2">Leadframe thickness without plating</td><td>c1</td><td>0.117</td><td>0.127</td><td>0.137</td></tr>
<tr><td rowspan="2">Outer Lead Distance</td><td>X</td><td>D</td><td>8.80</td><td>9.00</td><td>9.20</td></tr>
<tr><td>Y</td><td>E</td><td>8.80</td><td>9.00</td><td>9.20</td></tr>
<tr><td rowspan="2">Package size</td><td>X</td><td>D1</td><td>6.90</td><td>7.00</td><td>7.10</td></tr>
<tr><td>Y</td><td>E1</td><td>6.90</td><td>7.00</td><td>7.10</td></tr>
<tr><td colspan="2">Lead pitch</td><td>e</td><td>0.40</td><td>0.50</td><td>0.60</td></tr>
<tr><td colspan="2">H</td><td>H</td><td>8.14</td><td>8.17</td><td>8.20</td></tr>
<tr><td colspan="2">L</td><td>L</td><td>0.50</td><td>—</td><td>0.70</td></tr>
<tr><td colspan="2">Lead length</td><td>L1</td><td colspan="3">1.00 REF</td></tr>
<tr><td colspan="2">R1</td><td>R1</td><td>0.08</td><td>—</td><td>—</td></tr>
<tr><td colspan="2">R2</td><td>R2</td><td>0.08</td><td>—</td><td>0.20</td></tr>
<tr><td colspan="2">S</td><td>S</td><td>0.20</td><td>—</td><td>—</td></tr>
<tr><td colspan="2">Angle 1</td><td>Θ</td><td>0°</td><td>3.5°</td><td>7°</td></tr>
<tr><td colspan="2">Angle 2</td><td>Θ1</td><td>11°</td><td>12°</td><td>13°</td></tr>
<tr><td colspan="2">Angle 3</td><td>Θ2</td><td>11°</td><td>12°</td><td>13°</td></tr>
</table>

[1] Dimensions are expressed in millimeters.

Device Marking for LQFP48-EP

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

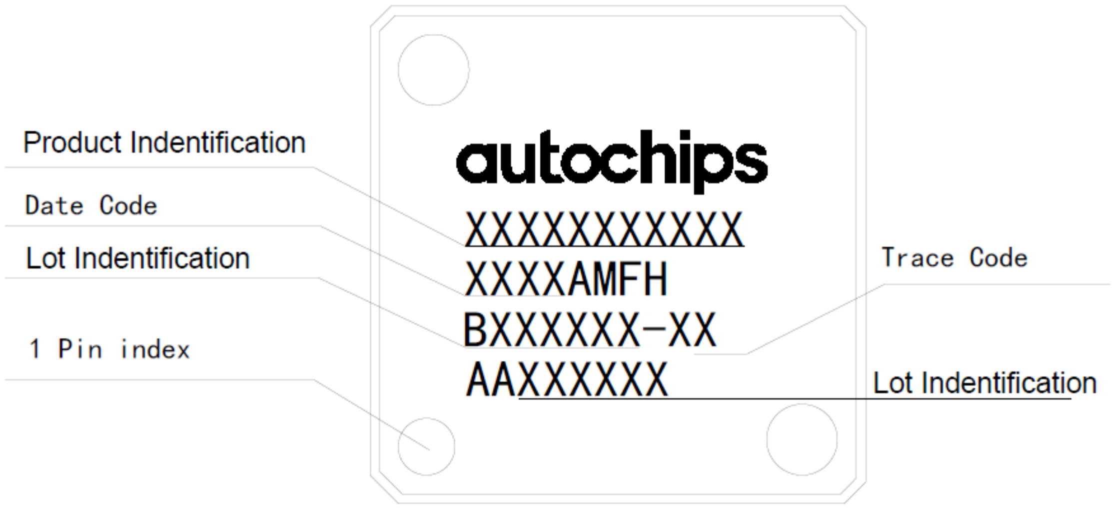

Figure 8-2 LQFP48-EP marking example (package top view)

9 Pinout

9.1 Signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

Table 9-1 Signal multiplexing and pin assignments [2]

48 PIN LQFP -EP	Pin Name	Function 0	Function 1	Function 2	Function 3	PINMUX	GPIO
1	PB11	gpio	PWM0_CH3	gpio	SPI1_MOSI	PMUX2[23:21]	27
2	PB12	gpio	PWM0_CH2	gpio	SPI1_SCK	PMUX2[26:24]	28
3	PB0	gpio	CAN_TX	PWM0_CH7	SPI1_MISO	PMUX1[20:18]	16
4	PB1	gpio	CAN_RX	PWM0_CH6	SPI1_NSS	PMUX1[23:21]	17
5	VDD1						
6	VSS1						
7	PA12	gpio	I2C0_SCL	OSC_OUT [1]	PWM0_FLT0	PMUX1[8:6]	12
8	PA15	gpio	I2C0_SDA	OSC_IN [1]	PWDT0_IN0	PMUX1[17:15]	15
9	PA0	gpio	PWM0_CH1	UART0_RTS	I2C0_SCL	PMUX0[2:0]	0
10	PA1	gpio	PWM0_CH0	UART0_CTS	I2C0_SDA	PMUX0[5:3]	1
11	PB3	gpio	PWM0_CH6	PWM1_CH7	SPI0_MOSI	PMUX1[29:27]	19
12	PA2	gpio	PWM0_CH5	ADC_IN8	SPI0_MISO	PMUX0[8:6]	2
13	PA3	gpio	PWM0_CH4	ADC_IN7	SPI0_SCK	PMUX0[11:9]	3

14	PA4	gpio	PWM0_CH3	ADC_IN6/ACMP_IN6	UART1_TX	PMUX0[14:12]	4
15	PA5	gpio	PWM0_CH2	ADC_IN5/ACMP_IN5	UART1_RX	PMUX0[17:15]	5
16	PA6	gpio	BOOT [1]	gpio		PMUX0[20:18]	6
17	PB15	gpio	PWM1_FLT0	ADC_IN11	SPI1_SCK	PMUX3[5:3]	31
18	PC0	gpio	PWM1_CH3	ADC_IN10	SPI1_MISO	PMUX3[8:6]	32
19	PC1	gpio	PWM1_CH2	ADC_IN9	SPI1_NSS	PMUX3[11:9]	33
20	PA7	gpio	UART0_TX	ADC_IN4/ACMP_IN4	SPI0_MOSI	PMUX0[23:21]	7
21	PA8	gpio	UART0_RX	ADC_IN3/ACMP_IN3	SPI0_NSS	PMUX0[26:24]	8
22	VCC_O						
23	VSS2						
24	VBAT						
25	VSS3						
26	EN						
27	RSTN						
28	VSS4						
29	LIN						
30	VSS5						
31	TXD(PC2) [3]	gpio	UART1_TX		UART0_TX	PMUX3[14:12]	34
32	RXD(PC3) [3]	gpio	UART1_RX		UART0_RX	PMUX3[17:15]	35
33	PA9	gpio	PWM0_FLT0	ADC_IN2/ACMP_IN2	RTC_CLKIN	PMUX0[29:27]	9

34	VDD2						
35	PB7	gpio	PWM1_CH3	ACMP_IN3	I2C0_SCL	PMUX2[11:9]	23
36	PB8	gpio	PWM1_CH2	PWDT0_IN2	I2C0_SDA	PMUX2[14:12]	24
37	PA10	gpio	PWM0_CH7	ADC_IN1/ACMP_IN1	PWDT0_IN2	PMUX1[2:0]	10
38	PA11	gpio	PWM0_CH6	ADC_IN0/ACMP_IN0	PWDT0_IN1	PMUX1[5:3]	11
39	PC6	gpio	UART1_TX	gpio	PWDT1_IN2	PMUX3[26:24]	38
40	PC7	gpio	UART1_RX	gpio	PWDT1_IN1	PMUX3[29:27]	39
41	PC8	gpio	PWM1_CH7	CAN_STDBY	PWDT1_IN0	PMUX4[2:0]	40
42	PC9	gpio	PWM1_CH6	gpio	ACMP_OUT	PMUX4[5:3]	41
43	PB9	gpio	PWM1_CH5	I2C1_SCL	UART2_TX	PMUX2[17:15]	25
44	PB10	gpio	PWM1_CH4	I2C1_SDA	UART2_RX	PMUX2[20:18]	26
45	PB2	gpio	NMI_B [1]	PWM0_FLT0	PWDT0_IN0	PMUX1[26:24]	18
46	PA13	gpio	SWD_CLK [1]	EXT_CLKIN	RTC_CLKOUT	PMUX1[11:9]	13
47	RESET_B	RESET_B					
48	PA14	gpio	SWD_DIO [1]	ACMP_OUT	PWM1_CH0	PMUX1[14:12]	14

[1] This functions as default function.

[2] All the pins are default as gpio on the first time power on except some dedicated pins.

For example, if we want to configure PIN1(PB11) as PWM0_CH3, we should set PMUX2[23:21] = 1.

[3] TXD and RXD are only used for TXD and RXD of LIN PHY. They are connected to PC2 and PC3 inside the chip respectively, and the external pins need NC.

9.2 Device pin assignment

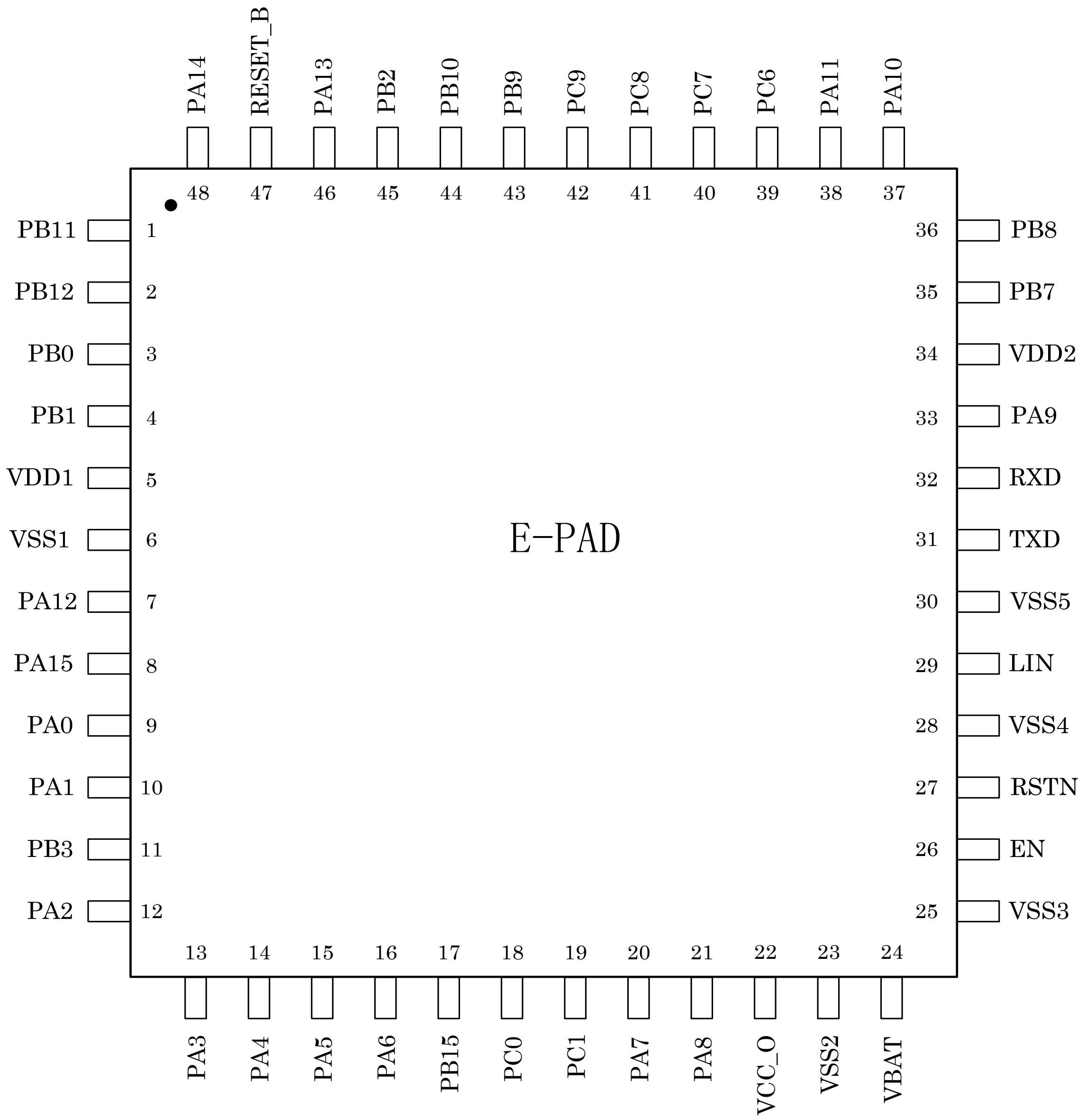

Figure 9-1 48-pin LQFP-EP package