AC7803x Data Sheet

Supports the following:

AC78036HFLA，AC78036FFLA，AC78036HELA，
AC78036FELA，AC78036HDLA，AC78036FDLA

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Revision	Date	Author	Description
1.0.0	2024-06-17	AutoChips	Official version
1.0.1	2025-03-28	AutoChips	Modify silkscreen information.

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1 Key features

- **Automotive grade**
  - AEC-Q100 Grade 1 qualified
- **Performance**
  - Up to 64 MHz ARM®Cortex-M0+ core
  - Single cycle 32-bit multiplier
  - Fast I/O access port
- **Memories and memory interfaces**
  - Two 256 KB Flash with ECC (256KB DFlash and 256KB PFlash)
  - 64 KB SRAM with ECC
- **Clocks**
  - External High Speed Oscillator(HFXOSC) - supports 8 MHz to 30 MHz crystal resonator; choice of low power or high gain oscillators
  - External Low Speed Oscillator (LFXOSC)
  - Internal Clock Source(LFOSC)—internal RC oscillator provides 8 MHz clock source
  - Internal 32 kHz low-power oscillator (LPO)
  - Internal PLL
- **System peripherals**
  - System Power management module (SPM) with three power modes: run mode , stop mode, standby mode
  - Low-voltage detection with reset (LVD)
  - Watchdog with independent clock source(WDG)
  - Serial wire debug (SWD) interfaces
- **Human-machine interface**
  - Up to 58 general-purpose input/output (GPIO)
  - External interrupt module is supported (IRQ)
- **Analog modules**
  - One up to 19-channel 12-bit 0.8Msps SAR ADC, optional hardware trigger (ADC)
  - One analog comparators containing a 8-bit DAC and programmable reference input(ACMP)
- **Timers**
  - Two 4-chaneel and one 8-channel complementary PWM
  - One 4-channel 32-bit periodic interrupt timer (TIMER)
  - Two pulse width timer (PWDT)
  - One real-time clock(RTC)

- **Communication interfaces**
  - Three UART modules (All support Software LIN)
  - Two SPI modules (SPI)
  - Two I2C modules (I2C)
  - Two CAN-FD modules, compatible with CAN
  - One EIO module(Enhanced IO)

- **Operating characteristics**
  - Voltage range：2.7 到 5.5 V
  - Temperature range(ambient): -40 to 125°C

- **Package options**
  - 64-pin LQFP
  - 48-pin LQFP

- **Information safety&Functional safety**
  - Low-voltage detection circuit with reset(LVD)
  - Programmable voltage detection (PVD)
  - Programmable CRC
  - Memory Protection Unit(MPU)
  - Clock Monitoring Unit(CMU)
  - Watchdog with independent clock source(WDG)
  - 128-bit unique ID

2 Block diagram

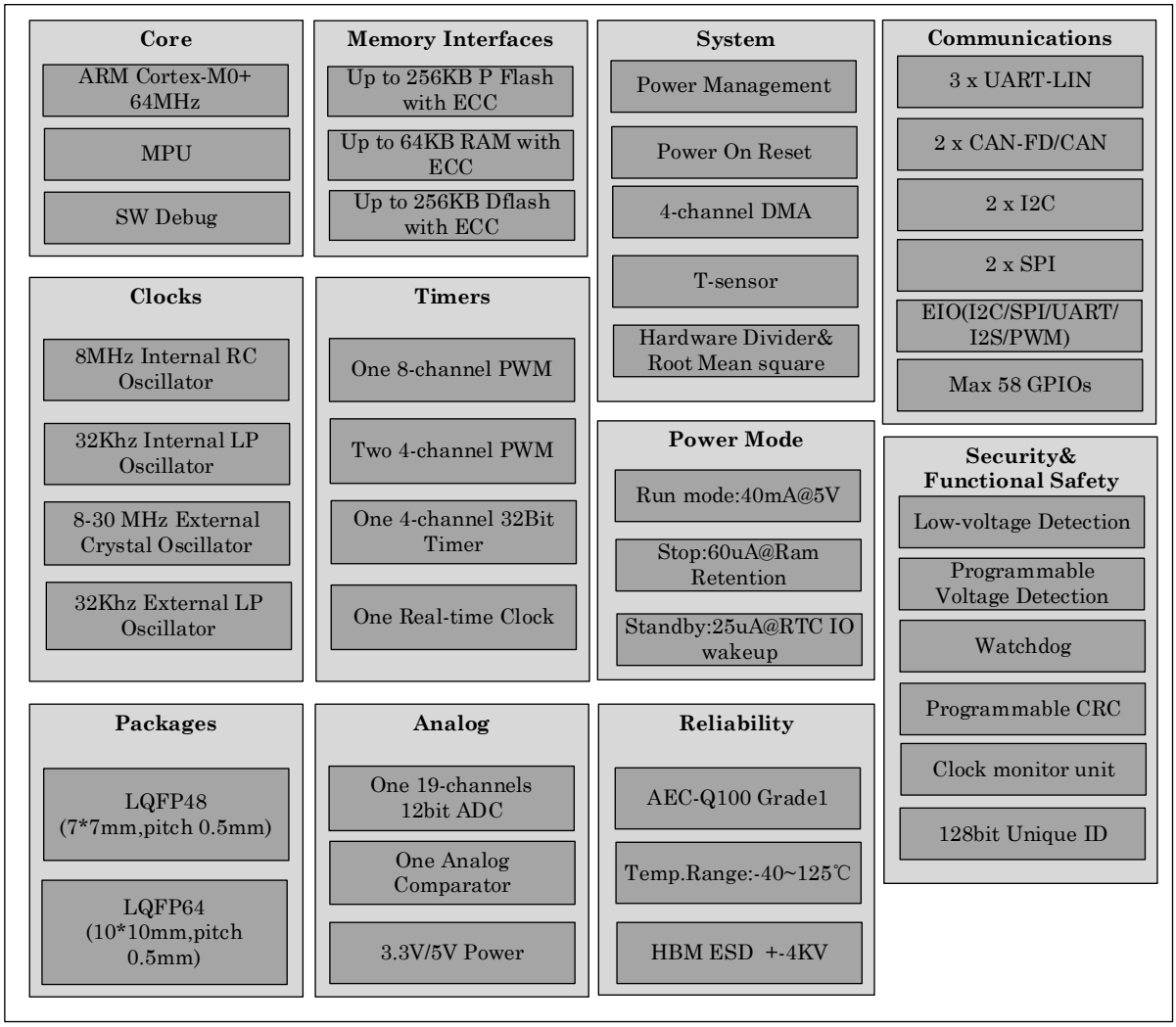

Figure 2-1 AC7803x block diagram

3 Part identification

3.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

3.2 Format

Part numbers for this device have the following format:

AC## HFLA

3.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Table 3-1 Fields

Field	Description	Values
AC	AutoChips	• AC
7	AutoChips mcu family	• 7
8	General Purpose Automotive MCU	• 8
0	Core Platform	• 0 = Cortex-M0+
3 6	Specific Function Bit	• 3: Product family • 6: Product subfamily
H	Pin Count	• P : 20 • M : 32 • F : 48 • H : 64 • L : 100 • Y : 144 • U : 176
F	Flash Memory Size	• A = 16KB • B = 32KB • C = 64KB • D = 128KB • E = 256KB • Z = 448KB • F = 512KB
L	Package type	• L = LQFP • Q = QFN • T = TSSOP
A	Temperature range(°C)	• A = AEC-Q100 Grade 1(-40~125°C) • I = -40~105°C C= -40~85°C
/x	Internal identification, only the packaging P/N suffix is used	/A or /B and so on

3.4 Example

This is an example part number: AC78036HFLA.

4 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate.

Table 4-1 Parameter classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

5 Ratings

5.1 Thermal handling ratings

Table 5-1 Thermal handling ratings

Symbo	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, High Temperature Storage Life.
2. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

5.2 Moisture handling ratings

Table 5-2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

5.3 ESD handling ratings

Table 5-3 ESD handling ratings

Symbol	Description	Min.	Max	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	–4000	4000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	–750	750	V	2
I_{LAT}	Latch-up current at ambient temperature of 125°C	–100	100	mA	3

1. Determined according to AEC-Q100-002-D, HUMAN BODY MODEL ELECTROSTATIC DISCHARGE TEST.

2. Determined according to AEC-Q100-011-C1, CHARGED DEVICE MODEL (CDM) ELECTROSTATIC DISCHARGE TEST.

3. Determined according to AEC-Q100-004-D, IC LATCH-UP TEST.

- Test was performed at 125 °C case temperature (Class II).
- Supply groups pass 1.5 $V_{ccmax.}$

5.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in the following table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this document.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pullup resistor associated with the pin is enabled.

Table 5-4 Voltage and current operating ratings

Symbo	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	2.7	5.5	V
I_{DD}	Maximum current into V_{DD}	—	60	mA
V_{IN}	Input voltage except true open drain pins	–0.3	V_{DD} + 0.3 [1]	V
	Input voltage of true open drain pins	–0.3	V_{DD} + 0.3 [1]	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins).	–16	16	mA

[1] Maximum rating of V_{DD} also applies to V_{IN}.

6 General

6.1 Nonswitching electrical specifications

6.1.1 Power and ground pins

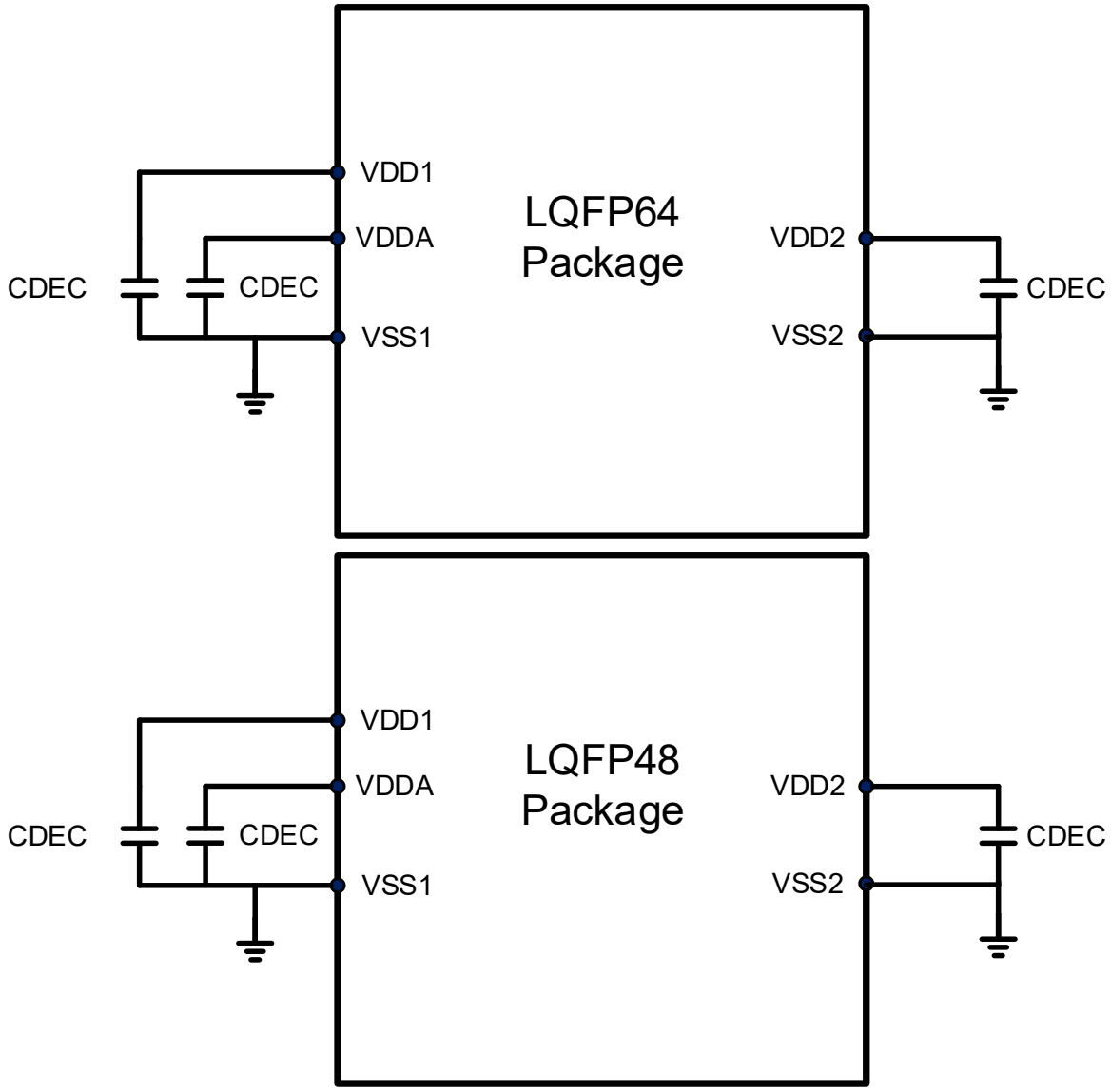

Figure 6-1 Pinout decoupling

1. V_{DD1} and V_{DD2} must be shorted to a common source on PCB.
2. All decoupling capacitors must be low ESR ceramic capacitors(X7R type), the recommended value is 0.1 uF.

3. For improved performance, it is recommended to use 10 uF, 0.1 uF and 1 nF capacitors in parallel.
4. All decoupling capacitors should be placed as close as possible to the corresponding power and ground pins.

6.1.2 DC characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 6-1 DC characteristics

Symbol	C	Descriptions			Min.	Typ.	Max.	Unit
—	—	Operating voltage		—	2.7	—	5.5	—
V_{OH}	P	Output high voltage	drive strength	5 V, I_{load} = -4, -8, -12, -16mA	V_{DD}-0.8	—	—	V
	C			3 V, I_{load} = –3.6, -7.2,-10.8,-14.4 mA	V_{DD}-0.8	—	—	V
I_{OHT}	D	Output high current	Max total I_{OH} for all ports	2.7≤V_{DD}<5.5 V	—	—	50	mA
V_{OL}	P	Output low voltage	drive strength	5 V, I_{load} = 4, 8, 12, 16mA	—	—	0.8	V
	C			3 V, I_{load} = 3.6, 7.2,10.8,14.4 mA	—	—	0.8	V
I_{OLT}	D	Output low current	Max total I_{OL} for all ports	2.7≤V_{DD}<5.5 V	—	—	50	mA
V_{IH}	P	Input high voltage	All digital inputs	4.5≤V_{DD}<5.5 V	0.65×V_{DD}	—	V_{DD} + 0.3	V
				2.7≤V_{DD}<4.5 V	0.70×V_{DD}	—	V_{DD} + 0.3	
V_{IL}	P	Input low voltage	All digital inputs	4.5≤V_{DD}<5.5 V	-0.3	—	0.35×V_{DD}	V
				2.7≤V_{DD}<4.5 V	-0.3	—	0.30×V_{DD}	
V_{hys}	C	Input hysteresis	All digital inputs	—	0.06×V_{DD}	—	—	V
I_{In}	P	Input leakage current	Per pin (pins in high impedance input mode)	V_{IN} = V_{DD} or V_{SS}	-1	0.1	1	uA

R_{PU}	P	Pullup resistors	All digital inputs, when enabled	—	40	75	150	kΩ
R_{PD}	P	Pulldown resistors	All digital inputs, when enabled	—	40	75	150	kΩ
I_{IC}	D	DC injection current	Single pin limit	$V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$	-2	—	2	mA
			Total MCU limit, includes sum of all stressed pins		-5	—	30	
C_{In}	C	Input capacitance, all pins		—	—	5	7	pF
V_{RAM}	C	RAM retention voltage		—	2.3	—	—	V

Table 6-2 LVD /POR / AVDD Voltage warning specification

Symbol	C	Description	Min.	Typ.	Max.	Unit
V_{POR}	D	POR re-arm voltage [1]	1.9	2.1	2.3	V
V_{LVRL}	C	Falling low-voltage detect threshold—low range (LVDV= 0)	2.5	2.6	2.7	V
V_{LVRH}	C	Falling low-voltage detect threshold—high range (LVDV=1) [2]	4.2	4.3	4.4	V
V_{HYSLVR}	C	Low-voltage detect hysteresis [2]	—	50	—	mV
V_{LVDL}	C	Falling low-voltage warning threshold—low range	2.8	2.9	3.0	V
V_{LVDH}	C	Falling low-voltage warning threshold—high range	4.5	4.6	4.7	V
V_{HYSLVD}	C	Low-voltage detect hysteresis	—	50	—	mV
V_{BG}	P	Buffered bandgap output [3]	1.18	1.2	1.22	V

[1] Maximum is the highest voltage that POR is guaranteed.

[2] Hysteresis = rising thresholds - falling threshold.

[3] Voltage Factory trimmed at V_{DD} = 5.0 V, Temp = 25 °C.

6.1.3 Supply current characteristics

Table 6-3 Supply current characteristics

Power Mode	Symbol	Core/Bus Frequency	V_{DD} (V)	-40℃	25℃ [1]	85℃	105℃	125℃	Unit
LFOSC(8M)，all modules clocks enabled	RI_{DD}	8/8 MHz	5	3.783	3.931	4.237	4.517	4.858	mA
		8/8 MHz	3.3	3.77	3.929	4.234	4.486	4.823	
LFOSC(8M)，all modules clocks disabled	RI_{DD}	8/8 MHz	5	2.555	2.683	2.975	3.255	3.595	mA
		8/8 MHz	3.3	2.545	2.683	2.974	3.22	3.558	
LFOSC(8M)+PLL，all modules clocks enabled	RI_{DD}	64/32 MHz	5	21.33	22.07	22.89	23.25	23.73	mA
		64/32 MHz	3.3	21.24	22.05	22.82	23.22	23.59	
LFOSC(8M)+PLL，all modules clocks disabled	RI_{DD}	64/32 MHz	5	16.05	16.74	17.5	17.85	18.34	mA
		64/32 MHz	3.3	15.98	16.69	17.43	17.83	18.2	
XOSC+PLL，all modules clocks enabled	RI_{DD}	64/32 MHz	5	23.33	24.24	25.32	25.81	26.45	mA
		24/24 MHz		16.03	16.86	17.88	18.36	19	
		12/12 MHz		12.64	13.43	14.41	14.89	15.52	
		8/8 MHz		9.374	10.13	11.06	11.53	12.15	
		64/32 MHz	3.3	23.25	24.15	25.23	25.78	26.25	
		24/24 MHz		15.95	16.76	17.8	18.33	18.81	
		12/12 MHz		12.55	13.33	14.33	14.85	15.34	
		8/8 MHz		9.284	10.02	10.98	11.49	11.98	
XOSC+PLL，all modules clocks disabled;	RI_{DD}	64/32 MHz	5	17.7	18.59	19.61	20.08	20.73	mA
		24/24 MHz		12.15	12.97	13.93	14.39	15.04	
		12/12 MHz		10.49	11.29	12.23	12.69	13.33	
		8/8 MHz		7.812	8.57	9.471	9.925	10.56	
		64/32 MHz	3.3	17.61	18.48	19.52	20.03	20.56	
		24/24 MHz		12.06	12.86	13.84	14.35	14.88	
		12/12 MHz		10.41	11.19	12.14	12.65	13.18	
		8/8 MHz		7.726	8.47	9.388	9.878	10.41	
Stop mode ;HSI_8M (selectable inactive or active module keep active)	SI_{DD}	8/8 MHz	5	0.937	0.995	1.207	1.429	1.751	mA
		8/8 MHz	3.3	0.929	0.988	1.205	1.403	1.735	
Stop mode ;HSI_8M (some selectable inactive or active module keep active)	SI_{DD}	8/8 MHz	5	0.026	0.061	0.262	0.479	0.792	mA
		8/8 MHz	3.3	0.023	0.059	0.255	0.448	0.785	
Stop mode ;HSI_8M (selectable inactive or active module keep inactive)	SI_{DD}	8/8 MHz	5	0.026	0.061	0.262	0.477	0.791	mA
		8/8 MHz	3.3	0.023	0.06	0.254	0.447	0.786	

Standby mode(selectable inactive or active module keep active)	SI_{DD}	32K	5	0.016	0.027	0.083	0.145	0.242	mA
		32K	3.3	0.013	0.025	0.083	0.139	0.237	
Standby mode (selectable inactive or active module keep inactive)	SI_{DD}	32K	5	0.016	0.027	0.083	0.144	0.241	mA
		32K	3.3	0.013	0.024	0.082	0.139	0.237	

[1] Data in Typical column was characterized at 25 °C, V_{DD}=3.3/5.0 V is typical recommended value.

6.2 Switching specifications

6.2.1 Control timing

Table 6-4 Control timing

Num	C	Rating		Symbol	Min.	Typ. [1]	Max.	Unit
1	D	System and core clock (t_{sys} = 1/f_{Sys})		f_{Sys}	DC	—	64	MHz
2	P	Bus frequency(t_{cyc} = 1/f_{Bus})		f_{Bus}	DC	—	32[2]	MHz
3	P	Internal low power oscillator frequency		f_{LPO}	—	32	—	kHz
4	D	External reset pulse width [3]		t_{extrst}	1.5 × t_{sys}	—	—	s
5	D	IRQ pulse width	Run mode[4]	t_{ILIH}/ t_{IHIL}	1.5 × t_{sys}	—	—	s
	D		Stop mode [4]	t_{ILIH}/ t_{IHIL}	1.5 × t_{32k}	—	—	s
6	D	Port rise and fall time - Normal drive strength(load = 50 pF) [5]	—	t_{Rise}	—	10.2	—	ns
	D			t_{Fall}	—	9.5	—	ns
	D	Port rise and fall time - high drive strength(load = 50 pF) [5]	—	t_{Rise}	—	5.4	—	ns
	D			t_{Fall}	—	4.6	—	ns

[1] Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

[2] The maximum operating frequency of AC7803x series, please refer to the product selection table.

[3] This is the shortest pulse that is guaranteed to be recognized as a RESET_B pin request.

[4] This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized.

[5] Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature ranges -40 °C to 125 °C.

6.2.2 PWM module timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the PWM clock.

Table 6-5 PWM input timing

C	Function	Symbol	Min.	Max.	Unit
D	Timer clock frequency	f_{PWM}	—	32 M	Hz
D	Input capture pulse width	t_{ICPW}	1.5	—	t_{PWM} [1]

[1] $t_{PWM}=1/f_{PWM}$.

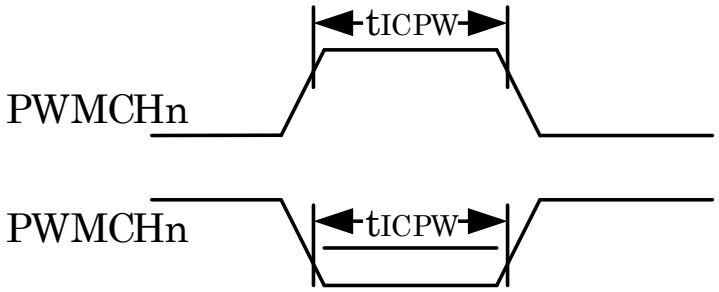

Figure 6-2 Timer input capture pulse

6.3 Thermal specifications

6.3.1 Thermal characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user- determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 6-6 Thermal characteristics

Board type	Symbol	Description	48 LQFP	64 LQFP	Unit	Notes
Dual-layer (1s1p)	θ_{JA}	Thermal resistance, junction to ambient (natural convection)	80.90	63.26	°C/W	1, 2

Four-layer (2s2p)	θ_{JA}	Thermal resistance, junction to ambient (natural convection)	51.23	44.90	°C/W	1, 3
Dual-layer (1s1p)	θ_{JMA}	Thermal resistance, junction to ambient (200 ft./min. air speed)	49.87	49.00	°C/W	1, 3
Four-layer (2s2p)	θ_{JMA}	Thermal resistance, junction to ambient (200 ft./min. air speed)	40.06	37.50	°C/W	1, 3
—	θ_{JB}	Thermal resistance, junction to board	23.14	26.28	°C/W	4
—	θ_{JC}	Thermal resistance, junction to case	15.88	11.82	°C/W	5
Dual-layer (1s1p)	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center(natural convection)	19.23	19.54	°C/W	6
Four-layer (2s2p)	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center(natural convection)	20.17	19.78	°C/W	6
Dual-layer (1s1p)	Ψ_{JB}	Thermal characterization parameter, junction to package top outside center(natural convection)	20.73	21.01	°C/W	7
Four-layer (2s2p)	Ψ_{JB}	Thermal characterization parameter, junction to package top outside center(natural convection)	21.76	21.83	°C/W	7

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
3. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

The average chip-junction temperature (T_J) in °C can be obtained from:

$T_J = T_A + (P_D \times \theta_{JA})$ Where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts - chip internal power

$P_{I/O}$ = Power dissipation on input and output pins - user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$P_D = K \div (T_J + 273\ °C)$

Solving the equations above for K gives: $K = P_D \times (T_A + 273\ °C) + \theta_{JA} \times (PD)^2$

where K is a constant pertaining to the particular part. K can be determined by measuring

P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving the above equations iteratively for any value of T_A.

7 Peripheral operating requirements and behaviors

7.1 Core modules

7.1.1 SWD electricals

Table 7-1 SWD full voltage range electrical

Symbol	Description	Min.	Max.	Unit
—	Operating voltage	2.7	5.5	V
J1	SWD_CLK frequency of operation • Serial wire debug	0	20	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall time	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	5	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	5	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	42	ns

7.2 External oscillator (OSC) and ICS characteristics

7.2.1 External high speed oscillator(HFXOSC) characteristics

Table 7-2 XOSC specifications (temperature range = -40 to 125 °C ambient)

Num	C	Characteristic	Symbol	Min.	Typ.	Max.	Unit
1	C	Crystal frequency	f_{hi}	8	—	30	MHz
2	D	Load capacitors	CL1, CL2	See Note [1]		—	—
3	D	Series resistor	Rs	—	0	—	KΩ
4	C	Crystal start-up time	t_{CST}	—	—	2. 5	ms

[1] For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors designed for high-frequency applications, and selected to match the requirements of the crystal. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the

series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

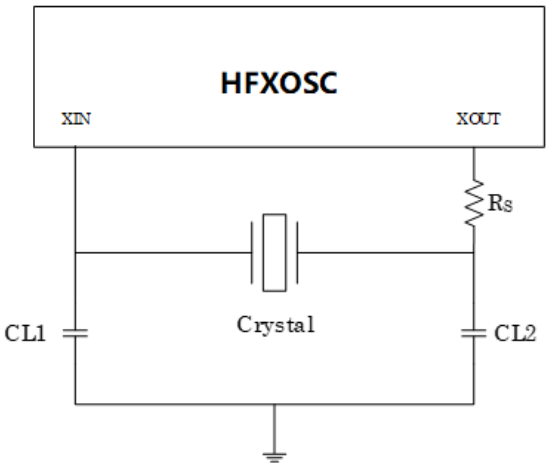

Figure 7-1 Typical crystal or resonator circuit

7.2.2 External low speed oscillator(LFXOSC) characteristics

Table 7-3 XOSC specifications (temperature range = -40 to 125 °C ambient)

Num	C	Characteristic	Symbol	Min.	Typ.	Max.	Unit
1	C	Crystal frequency	f_{hi}	—	32.768	—	KHz
2	D	Load capacitors	CL1, CL2	See Note [1]		—	
3	D	Series resistor	Rs	—	0	—	KΩ
4	C	Crystal start-up time	t_{CST}	—	—	500	ms

[1] For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors designed for high-frequency applications, and selected to match the requirements of the crystal. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

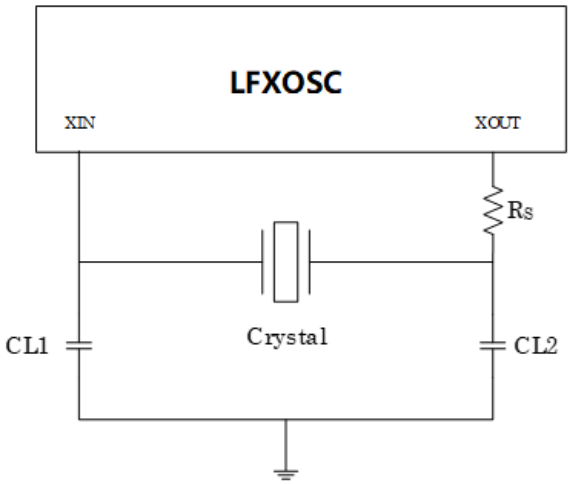

Figure 7-2 Typical crystal or resonator circuit

7.2.3 Internal RC characteristics

Table 7-4 OSC and ICS specifications (temperature range = -40 to 125 °C ambient)

Num	C	Characteristic		Symbol	Min.	Typ.	Max.	Unit
1	P	LFOSC output frequency range	Over temperature range from -40 °C to 125°C	f_{lfosc}	7.736	8	8.264	MHz
2	P	LFOSC at T = 25 °C, V_{DD} = 2.7~5.5 V	Over temperature range from -40 °C	Δf_{int_t}	-3.3	—	3.3	%
3	P	LPOSC Internal reference clock frequency, factory trimmed	T = 25 °C, V_{DD} = 5 V	f_{int_ft}	—	32	—	KHz
4	P	LPOSC Factory trimmed internal oscillator accuracy	Over temperature range from -40 °C to 125°C , V_{DD} = 5 V	Δf_{int_ft}	-10	—	10	%

7.2.4 PLL characteristics

Table 7-5 PLL characteristics

No.	Symbol	C	Parameter	Min.	Typ.	Max.
1	f_{PLL_IN}	PLL input clock frequency	4	—	48	MHz

No.	Symbol	C	Parameter	Min.	Typ.	Max.
2	f_{PLL_REF}	PLL reference clock frequency	—	—	12	MHz
3	f_{PLL_OUT}	PLL output clock frequency	8	—	192	MHz
4	f_{VCO_OUT}	VCO output frequency	400	—	1000	MHz
Operating temperature: -40~125°C $f_{PLL\_OUT} = f_{VCO\_OUT}$ /Postdiv, Postdiv can be 2,4,6,…,60,62. $f_{PLL\_REF} = f_{PLL\_IN}$ /Prediv, Prediv can be 1,2,4.						

7.3 Embedded Flash specifications

This section provides details about program/erase/read parameters and reliability features for the Flash memory.

Table 7-6 Embedded Flash characteristics

C	Characteristic	Symbol	Min.	Typ.	Max.	Unit
D	Supply voltage for program/erase at temperature from - 40°C to 125 °C	$V_{prog/erase}$	2.7	—	5.5	V
D	Supply voltage for read operation	V_{Read}	2.7	—	5.5	V
D	Flash Bus frequency	f_{SYS}	8	32	64	MHz
D	Time for Flash read once	t_{RDONCE}	4	4	6	t_{cyc}[1]
D	Mass Erase (all Main Block pages)	t_{MER}	—	12	—	ms
D	Page Erase (one page)	t_{PER}	—	5	—	ms
D	Mass Erase Verify	t_{MERV}	—	131081	—	t_{cyc}[1]
D	Page Erase Verify	t_{PERV}	—	521	—	t_{cyc}[1]
D	Program Flash (1 word)	t_{PRG1}	—	35	—	us
D	Program Flash (n word, n>1)	t_{PRGn}	—	35×n	—	us
C	Flash Program/erase endurance at temperature from - 40°C to 125 °C	n_{EDR}	10 k	—	—	times
C	Data retention time	t_{RET}	100@25℃ 20@105℃ 10@125℃	—	—	year

[1] $t_{cyc} = 1/ f_{SYS}$。

7.4 Analog

7.4.1 ADC characteristics

Table 7-7 12 bit ADC and Tsensor Operating Conditions and Characteristics

C	Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
D	V_{AVDD}	Supply Voltage	Absolute	2.7	—	5.5	V
D	V_{REFH}	Positive reference input[1]	Absolute	2.9	—	V_{AVDD}	V
D	V_{REFL}	Negative reference input	Absolute	—	0	—	V
D	V_{IN}	Input Voltage Range	Refer to the Supply Power	0	—	V_{AVDD}	**V**
D			Refer to the V_{REFH}	0	—	V_{REFH}	**V**
D	R_{IN}	Source impedance	Refer to the formula[2]	—	—	—	Ω
D	C_{ADC}	Internal Sampling Capacitor	—	—	2.02	—	pF
D	R_{ADC}	Sampling switch resistance	—	—	2.5	—	KΩ
D	f_{ADC}	ADC Clock Frequency	—	—	—	16	MHz
D	N_{sample}	Sampling Time	—	—	8	—	—
C	f_{trig}	Sampling frequency	f_{ADC}=16 MHz	—	—	0.8	MHz
C	INL	Integral Non-Linearity	—	—	±1.5	—	LSB [3]
C	DNL	Differential Non-Linearity	—	—	±1.5	—	LSB [3]
C	TUE	Total Unadjusted Error	—	-8	—	8	LSB [3]
P	CH	External Channels	—	—	—	19	—

[1] When using VREFH, AVDD≥VREFH is required.

[1] The relationship between input source impedance and sampling time must satisfy the formula: $R_{IN} < \frac{T_s}{f_{ADC} * C_{ADC} * ln(2^{N+2})} - R_{ADC}$, N is the ADC bits, ADC sampling duration must meet the settling accuracy of 0.25LSB, and the parasitic capacitance of the PAD terminal is not considered in the formula.

[2] Use the power as the ADC reference, LSB = V_{AVDD} /2^{12}, use V_{REFH} as the ADC reference, LSB = V_{REFH} /2^{12}.

Table 7-8 12 bit ADC and Tensors Operating Conditions and Characteristics(continue)

Characteristic	Conditions	C	Symbol	Min.	Typ.	Max.	Unit
Temp sensor slope	-40 °C~125 °C	D	Slope	—	2.6	—	mV/°C
Temp sensor voltage	25 °C	D	V_{TEMP25}	—	0.816	—	V

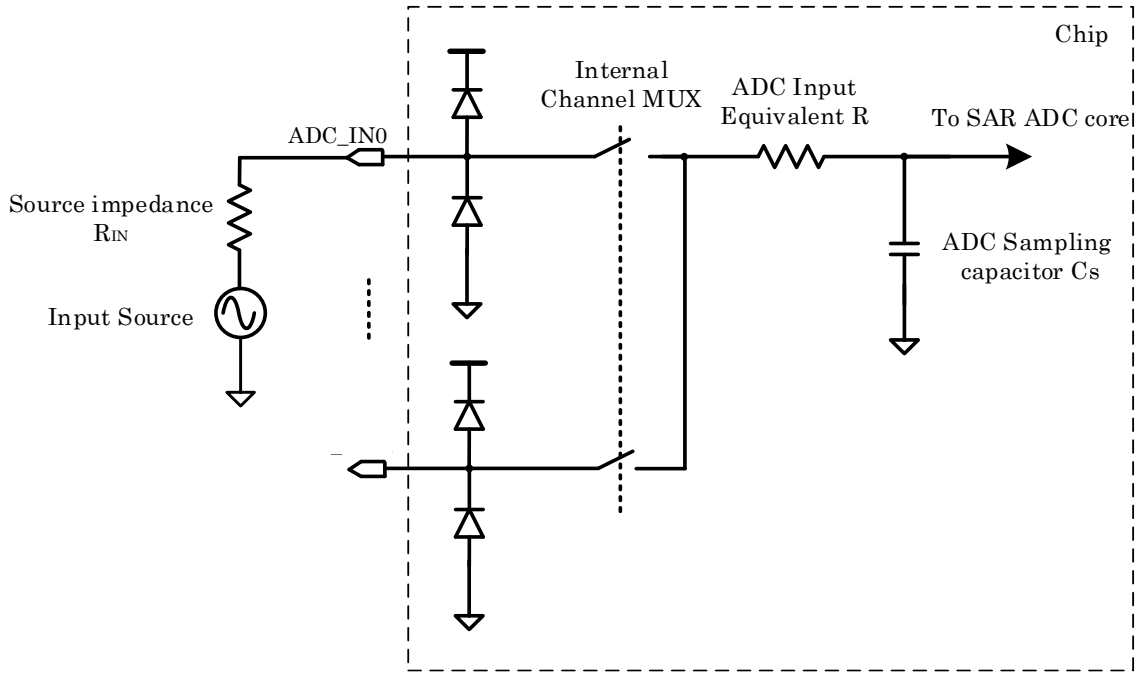

Figure 7-3 ADC input equivalent diagram

7.4.2 Analog comparator (ACMP) electricals

Table 7-9 Comparator electrical specifications

C	Characteristic	Condition	Symbol	Min.	Typ.	Max.	Unit
D	Supply voltage	—	V_{AVDD}	2.7	—	5.5	V
T	Supply current (Operation mode)	Only ACMP	I_{DDA}	—	—	25	μA
D	Analog input voltage	—	V_{AIN}	V_{SS}	—	V_{AVDD}	V
P	Analog input offset voltage[2]	—	V_{AIO}	-30	—	30	mV
C	Analog comparator hysteresis voltage[2]	No hysteresis	V_{HYS}	—	0	—	mV
C	Analog comparator hysteresis voltage[2]	Low hysteresis	V_{HYS}	—	10	—	mV
C	Analog comparator hysteresis voltage[2]	Middle hysteresis	V_{HYS}	—	20	—	mV

C	Analog comparator hysteresis voltage[2]	High hysteresis	V_{HYS}	—	40	—	mV
D	Supply current (off mode)	—	I_{DDAOFF}	—	—	100	nA
T	Propagation delay[2]	—	t_D	—	0.4	1[1]	µs
P	Digital-to-analog converter integration nonlinearity[3]	Vref=V_{AVDD}	INL	-1	—	1	LSB
P	Digital-to-analog converter integration nonlinearity[3]	Vref=V_{BG}	INL	-1	—	1	LSB
T	Digital-to-analog converter output	With buffer	DAC_OUT	0.2	—	V_{AVDD}-0.2	V
T	Digital-to-analog converter output	Without buffer	DAC_OUT	0.2	—	V_{AVDD}-0.2	V
D	Digital-to-analog converter load capacitance	—	C_{LOAD}	—	—	6	pF
D	Digital-to-analog converter static power consumption	Vref=5.5V	I_{DDA}	—	48.3	—	µA
D	Digital-to-analog converter static power consumption	Vref=V_{BG}	I_{DDA}	—	48.5	—	µA

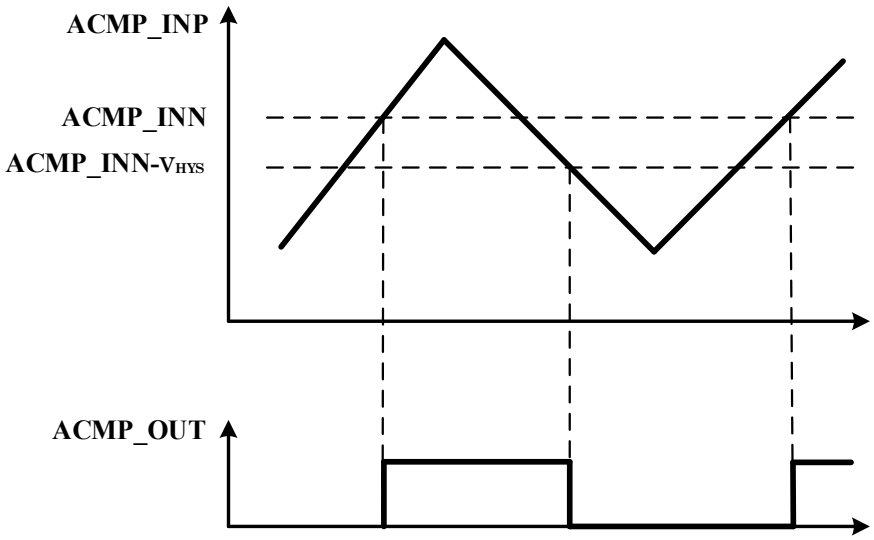

Figure 7-4 ACMP hysteresis diagram

[1] The ACMP input is connected to an external channel, with the filtering mode set to bypass.

[2] This test environment is when the input voltage =VAVDD /2.

[3] Without buffer.

7.5 Communication interfaces

7.5.1 SPI specifications

The serial peripheral interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's reference manual for information about the modified transfer formats used for communicating with slower peripheral devices.

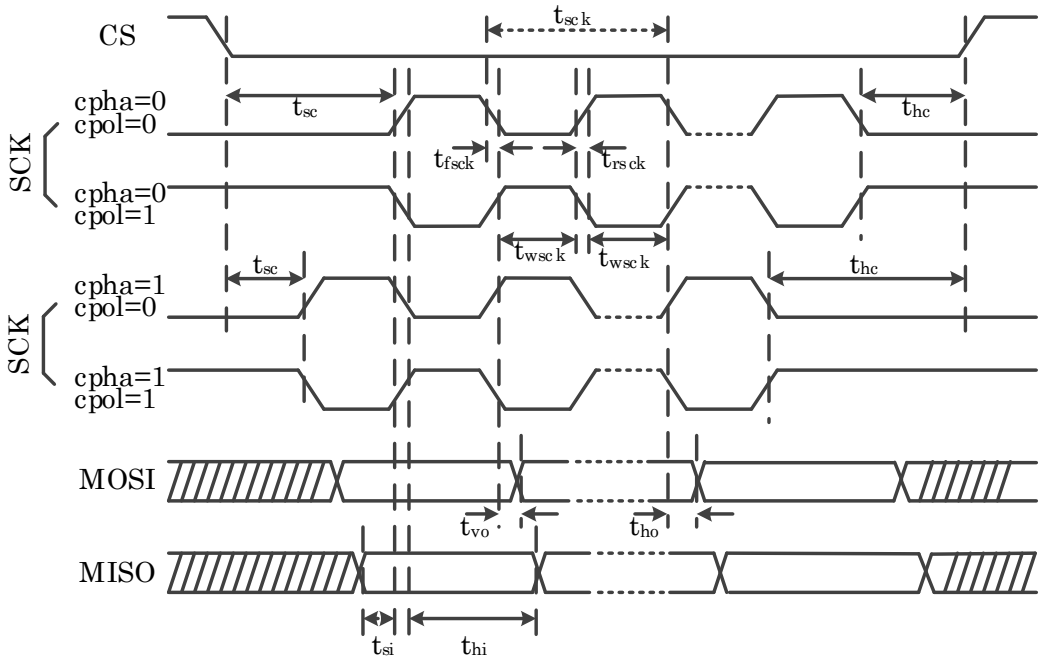

Figure 7-5 SPI timing diagram – master

Table 7-10 SPI characteristics – master

Symbol	Description	Min.	Max.	Unit	Comment
f_{op}	Frequency of operation	f_{bus}/512	12M	Hz	The maximum operating frequency can be half the value of the bus frequency (f_{bus}).
t_{sc}	CS setup time	1×t_{bus}	256×t_{bus}	ns	Negative edge of CS to first SCK edge
t_{hc}	CS hold time	1×t_{bus}	256×t_{bus}	ns	Last SCK edge to positive edge of CS
t_{wsck}	SCK high or low level time	1×t_{bus}	256×t_{bus}	ns	No considering **t_{rsck}** and **t_{fsck}**
t_{si}	Data input setup time	10	—	ns	—
t_{hi}	Data input hold time	10	—	ns	—

Symbol	Description	Min.	Max.	Unit	Comment
t_{vo}	Data output valid time	—	15	ns	—
t_{ho}	Data output hold time	-2	—	ns	—

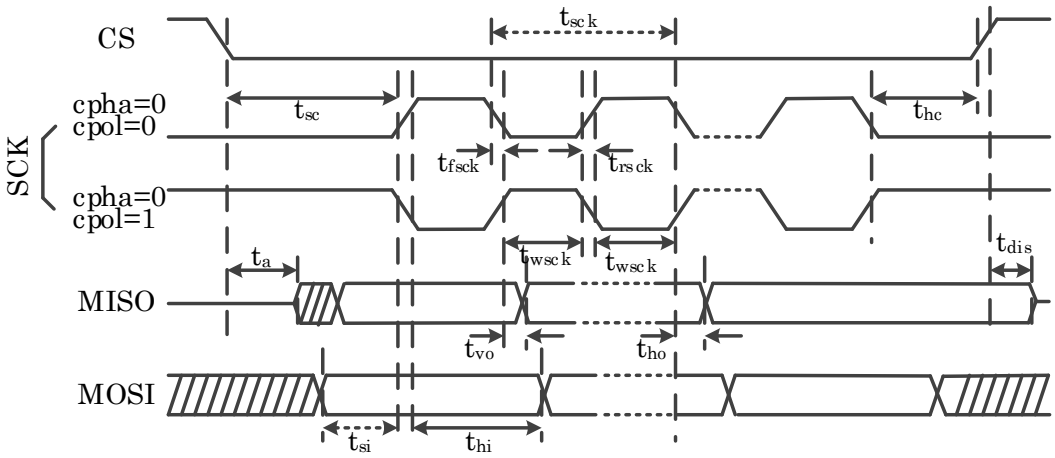

Figure 7-6 SPI timing diagram – slave(cpha=0)

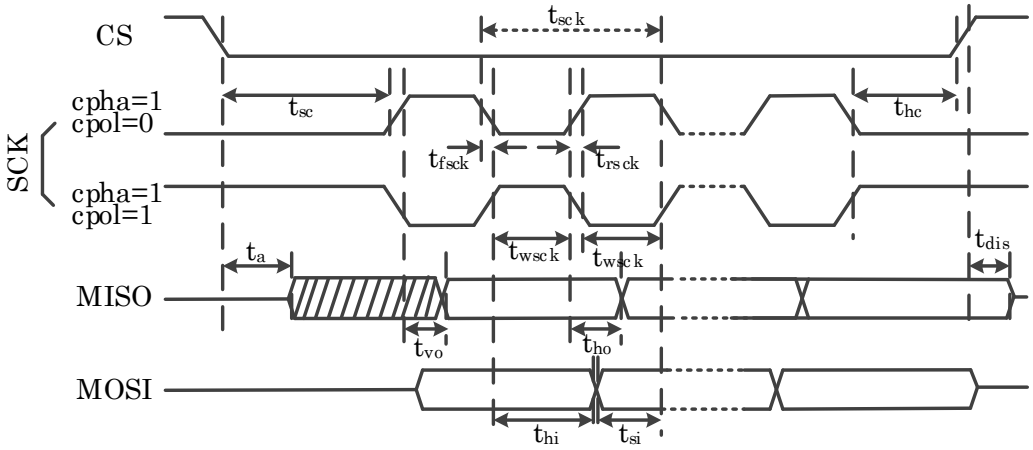

Figure 7-7 SPI timing diagram – slave(cpha=1)

Table 7-11 SPI characteristics - slave

Symbol	Description	Min.	Max.	Unit	Comment
f_{op}	Frequency of operation	—	12 M	Hz	Polling reception mode, with a maximum of 12M.
t_{sc}	CS setup time	$2\times t_{bus}$	—	ns	Negative edge of CS to first SCK edge
t_{hc}	CS hold time	$2\times t_{bus}$	—	ns	Last SCK edge to positive edge of CS

Symbol	Description	Min.	Max.	Unit	Comment
t_a	Slave access time	—	65	ns	Data from "Z" to effective
t_{dis}	Slave MISO disable time	—	65	ns	Data from effective to "Z"
t_{si}	Data input setup time	40	—	ns	—
t_{hi}	Data input hold time	20	—	ns	—
t_{vo}	Data output valid time	—	40	ns	—
t_{ho}	Data output hold time	22	—	ns	—

7.5.2 UART specifications

Basic function of Universal Asynchronous Receiver/Transmitter (UART) is to transmit and receive the serial data bit by bit. In order to support transmitting break field, sync field and data, additional Soft Local Interconnect Network(LIN) is included in the AC7803x chips. The main parameters of UART is introduced as below:

1. Up to three UART function channels and all of which support soft LIN functions (the uart function and LIN function of the same UART cannot be used at the same time).
2. UART can transmit or receive data with the range of baud rate from 600 bps to 4.2 Mbps.
3. The minimum GPIO pin interrupt pulse width is 333 ns. Because of that these pins do not have a passive filter on the inputs, this is the shortest pulse width that is guaranteed to be recognized.
4. The maximum baud rate supported in soft LIN function is 20 kbps.
5. Auto baud rate detection is selectable open or not in soft LIN function. The tolerance of received baud rate is from 50% to +100% · in this case.

7.5.3 CAN specifications

Table 7-12 CAN wake-up pulse characteristics

Symbol	Description	Min.	Typ.	Max.	Unit
CAN dominant wakeup pulse parameter filtered	tWUP	1.4	—	3.45	µs
CAN dominant wakeup pulse parameter effective	tWUP	—	2	—	µs

7.5.4 I2C specifications

Table 7-13 Characteristics of the I2C bus lines for different mode

Symbol	Parameter	Standard-mode		Fast-mode		Fast-mode Plus		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCL}	SCL clock frequency	0	100	0	400	0	1000	KHz
$t_{HD;STA}$	hold time START condition	4	—	0.6	—	0.26	—	µs
t_{LOW}	LOW period of the SCL clock	4.7	—	1.3	—	0.5	—	µs
t_{HIGH}	HIGH period of the SCL clock	4	—	0.6	—	0.26	—	µs
$t_{SU;STA}$	Set-up time for a repeated START condition	4.7	—	0.6	—	0.26	—	µs
$t_{HD;DAT}$	data hold time	0	—	0	—	0	—	µs
$t_{SU;DAT}$	data set-up time	250	—	100	—	50	—	ns
t_r	rise time of both SDA and SCL signals	—	1000	20	300	-	120	ns
t_f	fall time of both SDA and SCL signals	—	300	20 × (V_{DD} / 5.5 V)	300	20 × (V_{DD} / 5.5 V)	120	ns
$t_{SU;STO}$	set-up time for STOP condition	4	—	0.6	—	0.26	—	µs
t_{BUF}	bus free time between a STOP and START condition	4.7	—	1.3	—	0.5	—	µs
C_b	capacitive load for each bus line	—	400	—	400	—	550	pF
$t_{VD;DAT}$	data valid time	—	3.45	—	0.9	—	0.45	µs
$t_{VD;ACK}$	data valid acknowledge time	—	3.45	—	0.9	—	0.45	µs
V_{nL}	noise margin at the LOW level	0.1V_{DD}	—	0.1V_{DD}	—	0.1V_{DD}	—	V
V_{nH}	noise margin at the HIGH level	0.2V_{DD}	—	0.2V_{DD}	—	0.2V_{DD}	—	V

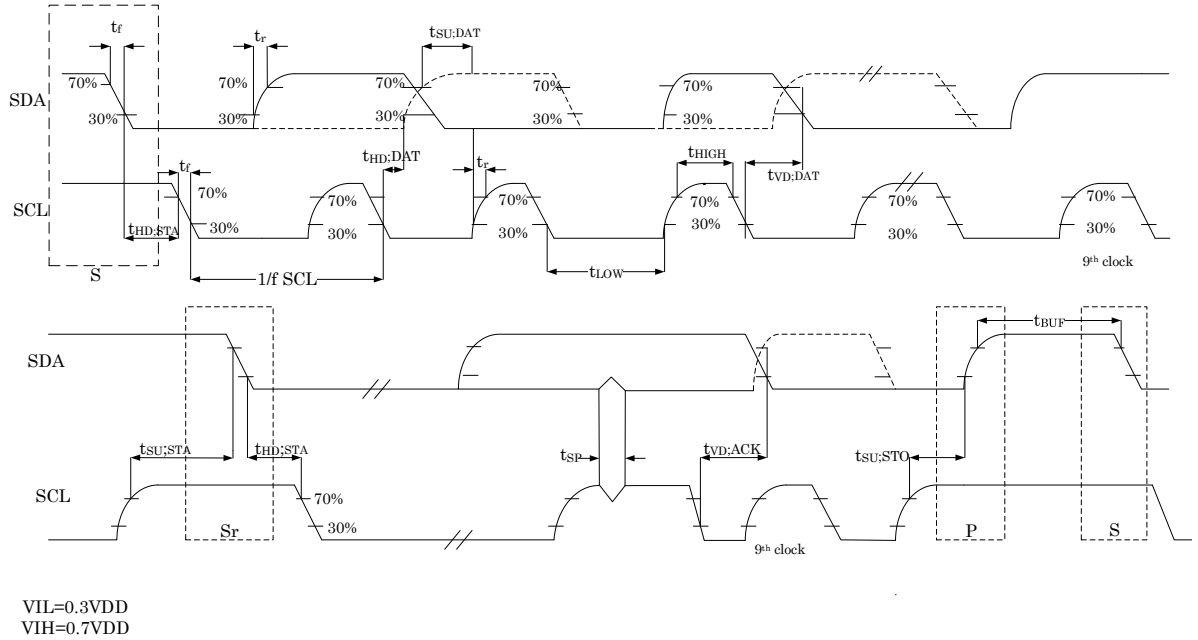

Figure 7-8 Definition of timing for F/S-mode devices on the I2C-bus

7.5.5 EIO specifications

EIO (Enhanced IO) is a highly configurable module that provides a wide range of functions, including:

- Emulate various serial communication protocols
- Four flexible 16-bit timers supporting trigger, reset, enable and disable conditions
- Four configurable 32-bit shifters supporting transmit, receive and match memory

With 4 timers and 4 shifters, the EIO module can support a wide range of protocols, including but not limited to:

- UART transmit and receive
- I2C master
- SPI master and slave
- I2S master and slave
- PWM waveform generation

8 Dimensions

8.1 LQFP48 package information

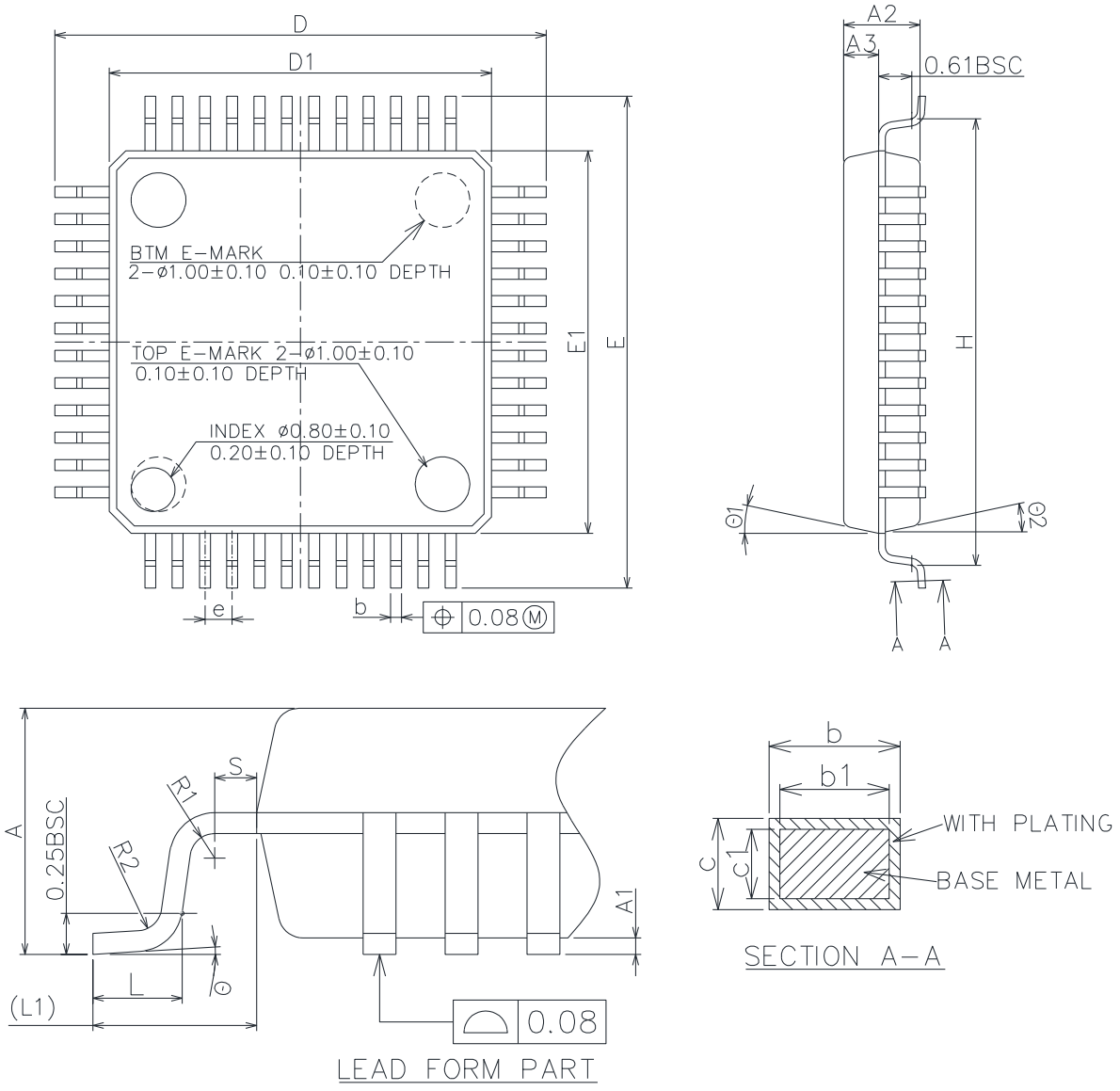

Figure 8-1 LQFP – 48 pin, 7 x 7 mm Low Profile Quad Flat Package Outline [1]

[1] Drawing is not to scale.

Table 8-1 LQFP – 48 pin，7 x 7 mm Low Profile Quad Flat Package Mechanical Data [1]

Item		Symbol	Min.	Nom.	Max.
Total height		A	—	—	1.60
Stand off		A1	0.05	—	0.15
Mold thickness		A2	1.35	1.40	1.45
Leadframe to mold height		A3	0.59	0.64	0.69
Lead width		b	0.18	—	0.27
Lead width without plating		b1	0.17	0.20	0.23
Leadframe thickness		c	0.13	—	0.18
Leadframe thickness without plating		c1	0.117	0.127	0.137
Outer lead distance	X	D	8.80	9.00	9.20
	Y	E	8.80	9.00	9.20
Package size	X	D1	6.90	7.00	7.10
	Y	E1	6.90	7.00	7.10
Lead pitch		e	0.40	0.50	0.60
H		H	8.14	8.17	8.20
L		L	0.50	—	0.70
Lead length		L1	1.00REF		
Lead forming arc radius		R1	0.08	—	—
R2		R2	0.08	—	0.20
θ		θ	0°	3.5°	7°
θ1		θ1	11°	12°	13°
θ2		θ2	11°	12°	13°

[1] Dimensions are expressed in millimeter.

LQFP48 device marking:

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

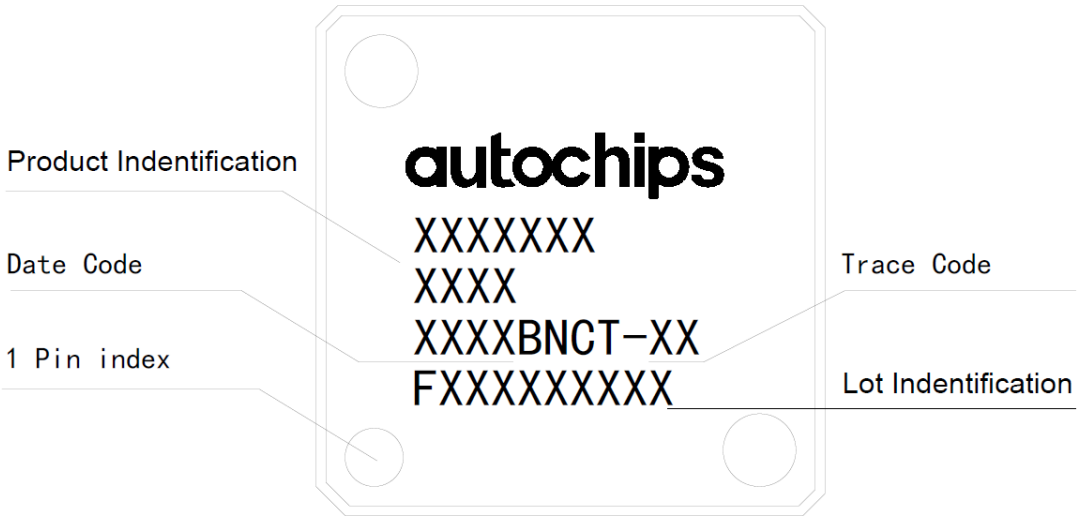

Figure 8-2 LQFP48 marking example (package top view)

8.2 LQFP64 package information

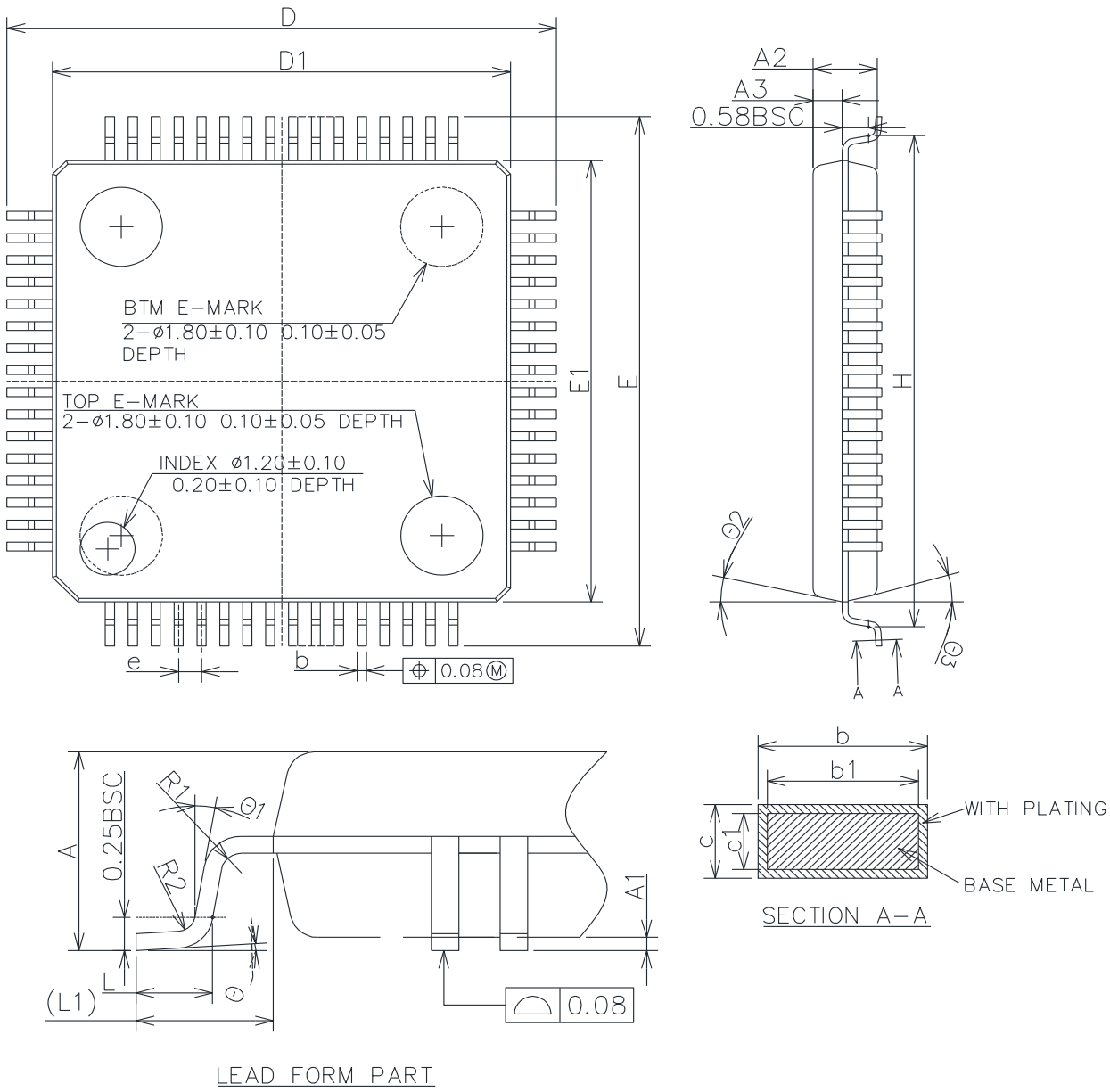

Figure 8-3 LQFP – 64 pin, 10 x 10 mm Low Profile Quad Flat Package Outline [1]

[1] Drawing is not to scale.

Table 8-2 QFP – 64 pin, 10 x 10 mm Low Profile Quad Flat Package Mechanical Data [1]

Item	Symbol	Min.	Nom.	Max.
Total height	A	—	—	1.60
Stand off	A1	0.05	—	0.15
Mold thickness	A2	1.35	1.40	1.45

Item		Symbol	Min.	Nom.	Max.
Leadframe to mold height		A3	0.59	0.64	0.69
Lead width		b	0.18	—	0.27
Lead width without plating		b1	0.17	0.20	0.23
Leadframe thickness		c	0.13	—	0.18
Leadframe thickness without plating		c1	0.117	0.127	0.137
Outer lead distance	X	D	11.95	12.00	12.05
	Y	E	11.95	12.00	12.05
Package size	X	D1	9.90	10.00	10.10
	Y	E1	9.90	10.00	10.10
Lead pitch		e	0.40	0.50	0.60
H		H	11.09	11.13	11.17
L		L	0.53	—	0.70
Lead length		L1	1.00REF		
Lead forming arc radius		R1	0.15REF		
R2		R2	0.13REF		
θ		θ	0°	3.5°	7°
θ1		θ1	0°	—	—
θ2		θ2	11°	12°	13°
θ3		θ3	11°	12°	13°

[1] Dimensions are expressed in millimeters.

LQFP64 device marking:

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

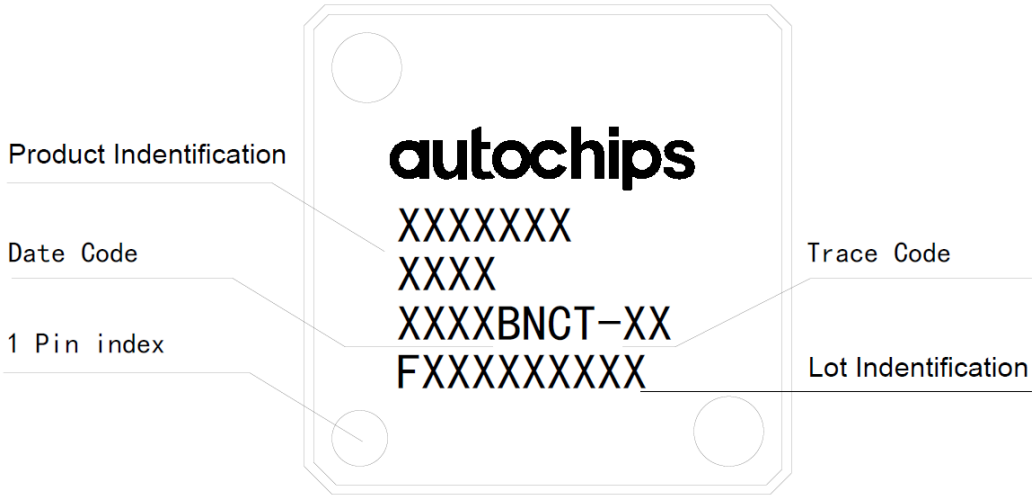

Figure 8-4 LQFP64 marking example (package top view)

9 Pin Assignments

9.1 Signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

Table 9-1 Signal multiplexing and pin assignments

48 PIN LQFP	64 PIN LQFP	AC7803 PAD	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6
1	1	PB11	GPIO	PWM0_CH3	SPI1_MISO	SPI1_MOSI	PWM2_CH1	EIO_D1	HIGH_Z
2	2	PB12	GPIO	PWM0_CH2		SPI1_SCK	PWM2_CH0	EIO_D0	HIGH_Z
	3	PC10	GPIO	SPI1_NSS	Timer_ALT0	PWM1_CH5		EIO_D5	HIGH_Z
	4	PC11	GPIO	CLKOUT		PWM1_CH4	CAN0_STDBY	EIO_D4	HIGH_Z
3	5	PB0	GPIO	CAN0_TX	PWM2_CH3	SPI1_MISO	OSC32_IN*AN	EIO_D7	HIGH_Z
4	6	PB1	GPIO	CAN0_RX	PWM2_CH2	SPI1_NSS	OSC32_OUT*AN	EIO_D6	HIGH_Z
5	7	VDD1							
6	8	VDDA							
	9	VREF+							
7	10	VSS1							
8	11	PA12	GPIO	I2C0_SCL	OSC_IN[1]	PWM0_FLT0			HIGH_Z
9	12	PA15	GPIO	I2C0_SDA	OSC_OUT[1]	PWDT0_IN0			HIGH_Z
	13	PC12	GPIO	PWM0_FLT0	UART2_RTS	PWM2_FLT0		ACMP_OUT	HIGH_Z
10	14	PA0	GPIO	PWM0_CH1	UART0_RTS	I2C0_SCL	SPI0_MISO	VREF-	HIGH_Z
11	15	PA1	GPIO	PWM0_CH0	UART0_CTS	I2C0_SDA	SPI0_SCK	VREF+	HIGH_Z
12	16	PB13	GPIO	PWM2_CH3	UART2_CTS	I2C1_SCL			HIGH_Z
13	17	PB3	GPIO	PWM2_CH2	PWM1_CH7	SPI0_MOSI	CAN1_STDBY	ACMP_IN8[1]	HIGH_Z
14	18	PA2	GPIO	PWM2_CH1	ADC_IN8[1]	SPI0_MISO	SPI0_NSS	CLKOUT	HIGH_Z
15	19	PA3	GPIO	PWM2_CH0	ADC_IN7[1]	SPI0_SCK	SPI0_MOSI	DAC_OUT	HIGH_Z
16	20	PA4	GPIO	PWM0_CH3	ADC_IN6/ACMP_IN6[1]	UART1_TX	CAN1_TX	UART0_TX	HIGH_Z
17	21	PA5	GPIO	PWM0_CH2	ADC_IN5/ACMP_IN5[1]	UART1_RX	CAN1_RX	UART0_RX	HIGH_Z
	22	PC13	GPIO	UART2_TX	ACMP_IN10[1]	PWM0_FLT0			HIGH_Z
	23	PC14	GPIO	UART2_RX	ACMP_IN11[1]	PWM2_FLT0			HIGH_Z
18	24	PA6	GPIO	BOOT[1]	Timer_ALT1	SPI0_NSS	PWM2_CH3	PWM2_FLT0	HIGH_Z
19	25	PB14	GPIO	PWM0_CH1	ADC_IN15[1]	SPI1_MOSI		PWM1_CH7	HIGH_Z
	26	PC15	GPIO	PWM0_CH0	ADC_IN16[1]	SPI1_MISO		PWM1_CH6	HIGH_Z
	27	PD0	GPIO	PWM1_FLT1	ADC_IN17[1]		CAN1_TX	UART2_TX	HIGH_Z
20	28	PB15	GPIO	PWM1_FLT0	ADC_IN11[1]	SPI1_SCK	CAN1_RX	UART2_RX	HIGH_Z
21	29	PC0	GPIO	PWM1_CH3	ADC_IN12[1]	SPI1_MISO	SPI1_SCK	CAN1_STDBY	HIGH_Z
22	30	PC1	GPIO	PWM1_CH2	ADC_IN13[1]	SPI1_NSS			HIGH_Z
23	31	PB4	GPIO	PWM1_CH1	ADC_IN9[1]	SPI0_MISO	PWM0_CH0	PWM2_CH2	HIGH_Z
24	32	PB5	GPIO	PWM1_CH0	ADC_IN10[1]	SPI0_SCK	PWM0_CH1	CAN0_STDBY	HIGH_Z
25	33	PA7	GPIO	UART0_TX	ADC_IN4/ACMP_IN4[1]	SPI0_MOSI	CAN0_TX	PWM1_CH5	HIGH_Z
26	34	PA8	GPIO	UART0_RX	ADC_IN3/ACMP_IN3[1]	SPI0_NSS	CAN0_RX	Timer_ALT2	HIGH_Z
27	35	PC2	GPIO	UART1_TX	PWM2_FLT0	UART0_TX	PWM1_CH0	UART0_RTS	HIGH_Z
28	36	PC3	GPIO	UART1_RX	PWM1_FLT1	UART0_RX	PWM1_CH1	UART0_CTS	HIGH_Z
29	37	PA9	GPIO	PWM2_FLT0	ADC_IN2/ACMP_IN2[1]	RTC_CLKIN	UART1_RTS	PWM1_CH3	HIGH_Z
	38	PD1	GPIO	PWM0_FLT0	ADC_IN18[1]	SPI1_NSS	UART1_CTS	PWM1_CH5	HIGH_Z
	39	PD2	GPIO	PWM1_CH7	PWM1_FLT0				HIGH_Z
30	40	VSS2							
31	41	VDD2							
32	42	PC4	GPIO	PWM0_CH1	ADC_IN14[1]	I2C1_SDA	CAN1_TX	PWM1_FLT1	HIGH_Z
	43	PD3	GPIO	PWM0_CH0	PWM1_FLT0		CAN1_RX		HIGH_Z
	44	PD4	GPIO	PWM0_FLT0	PWM1_FLT1		CAN1_STDBY		HIGH_Z
33	45	PB6	GPIO	PWM1_CH6	PWM1_FLT0	CAN0_STDBY	SPI1_NSS	EIO_D7	HIGH_Z
34	46	PC5	GPIO	PWM1_CH5	PWDT0_IN1	SPI0_NSS	SPI1_MOSI	EIO_D6	HIGH_Z
35	47	PB7	GPIO	PWM1_CH3	ACMP_IN7[1]	I2C0_SCL	UART0_TX	EIO_D5	HIGH_Z

36	48	PB8	GPIO	PWM1_CH2	PWDT0_IN2	I2C0_SDA	UART0_RX	EIO_D4	HIGH_Z
37	49	PA10	GPIO	PWM2_CH3	ADC_IN1/ACMP_IN1[1]	PWDT0_IN2	EIO_D3	UART0_RTS	HIGH_Z
38	50	PA11	GPIO	PWM2_CH2	ADC_IN0/ACMP_IN0[1]	PWDT0_IN1	EIO_D2	UART0_CTS	HIGH_Z
39	51	PC6	GPIO	UART1_TX	Timer_ALT0	PWDT1_IN2	CAN0_TX	PWM1_CH1	HIGH_Z
40	52	PC7	GPIO	UART1_RX	Timer_ALT1	PWDT1_IN1	CAN0_RX	PWM1_CH0	HIGH_Z
	53	PD5	GPIO	SPI0_NSS	PWM1_CH7	CAN0_STDBY	UART1_RTS		HIGH_Z
	54	PD6	GPIO	SPI0_MOSI	PWM1_CH6	Timer_ALT2	UART1_CTS		HIGH_Z
41	55	PC8	GPIO	PWM1_CH7	CAN0_STDBY	PWDT1_IN0	CAN1_TX	PWM2_CH0	HIGH_Z
42	56	PC9	GPIO	PWM1_CH6	Timer_ALT3	ACMP_OUT	CAN1_RX	PWM2_CH1	HIGH_Z
43	57	PB9	GPIO	PWM1_CH5	I2C1_SCL	UART2_TX	CAN1_STDBY	EIO_D1	HIGH_Z
44	58	PB10	GPIO	PWM1_CH4	I2C1_SDA	UART2_RX	PWDT1_IN0	EIO_D0	HIGH_Z
	59	PD7	GPIO	SPI0_MISO		SPI1_NSS	PWM1_FLT1		HIGH_Z
	60	PD8	GPIO	SPI0_SCK		SPI1_MOSI	PWM1_FLT0		HIGH_Z
45	61	PB2	GPIO[1]	NMI_B	PWM0_FLT0	PWDT0_IN0	PWM2_CH0	RTC_CLKOUT	HIGH_Z
46	62	PA13	GPIO	SWD_CLK[1]		RTC_CLKOUT	PWM1_CH0	ACMP_IN9	HIGH_Z
47	63	PD9	GPIO	RESET_B[1]					HIGH_Z
48	64	PA14	GPIO	SWD_DIO[1]	ACMP_OUT	PWM1_CH0			HIGH_Z

[1] This functions as default function.

9.2 Device pin assignment

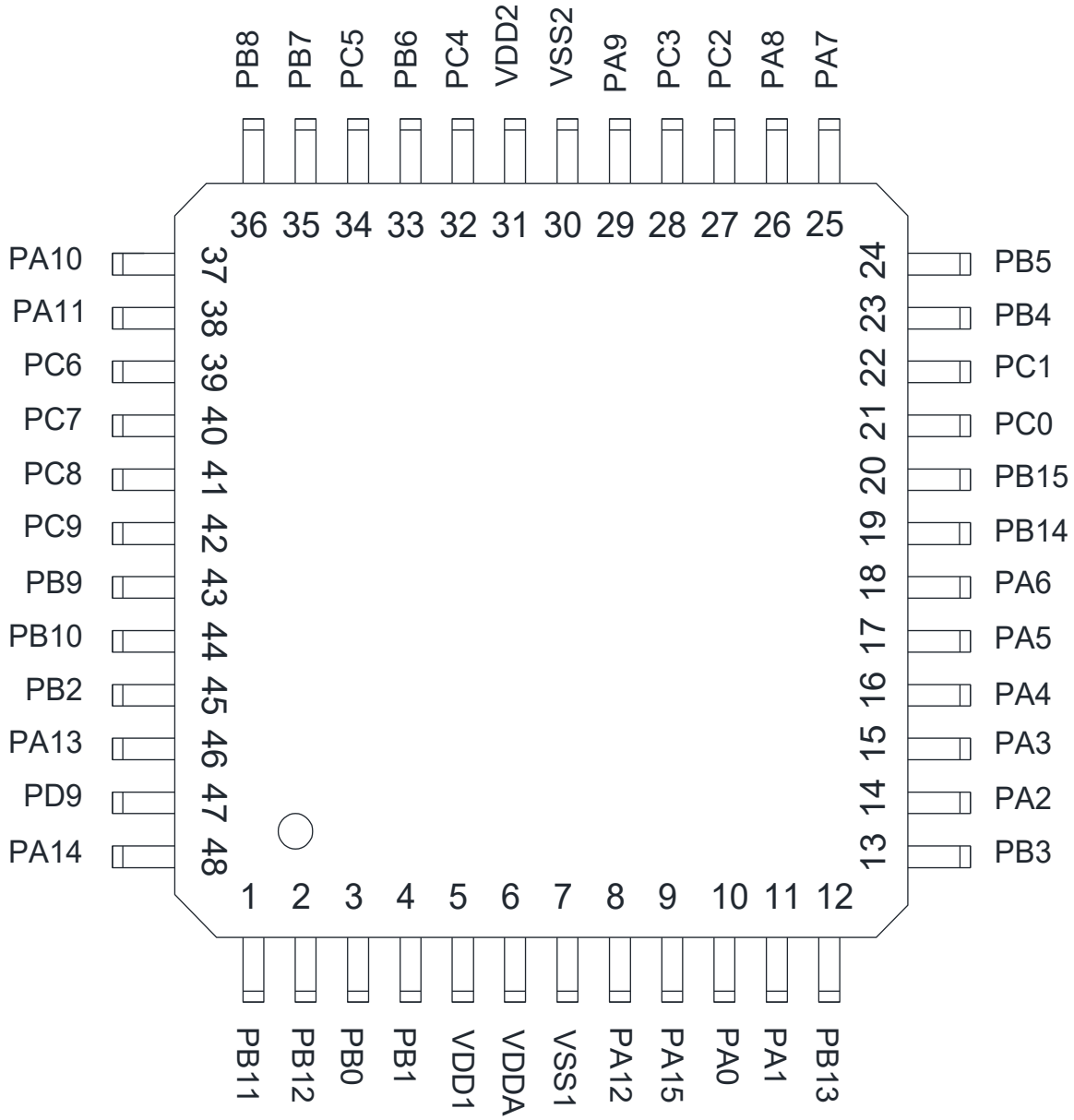

Figure 9-1 LQFP48 package

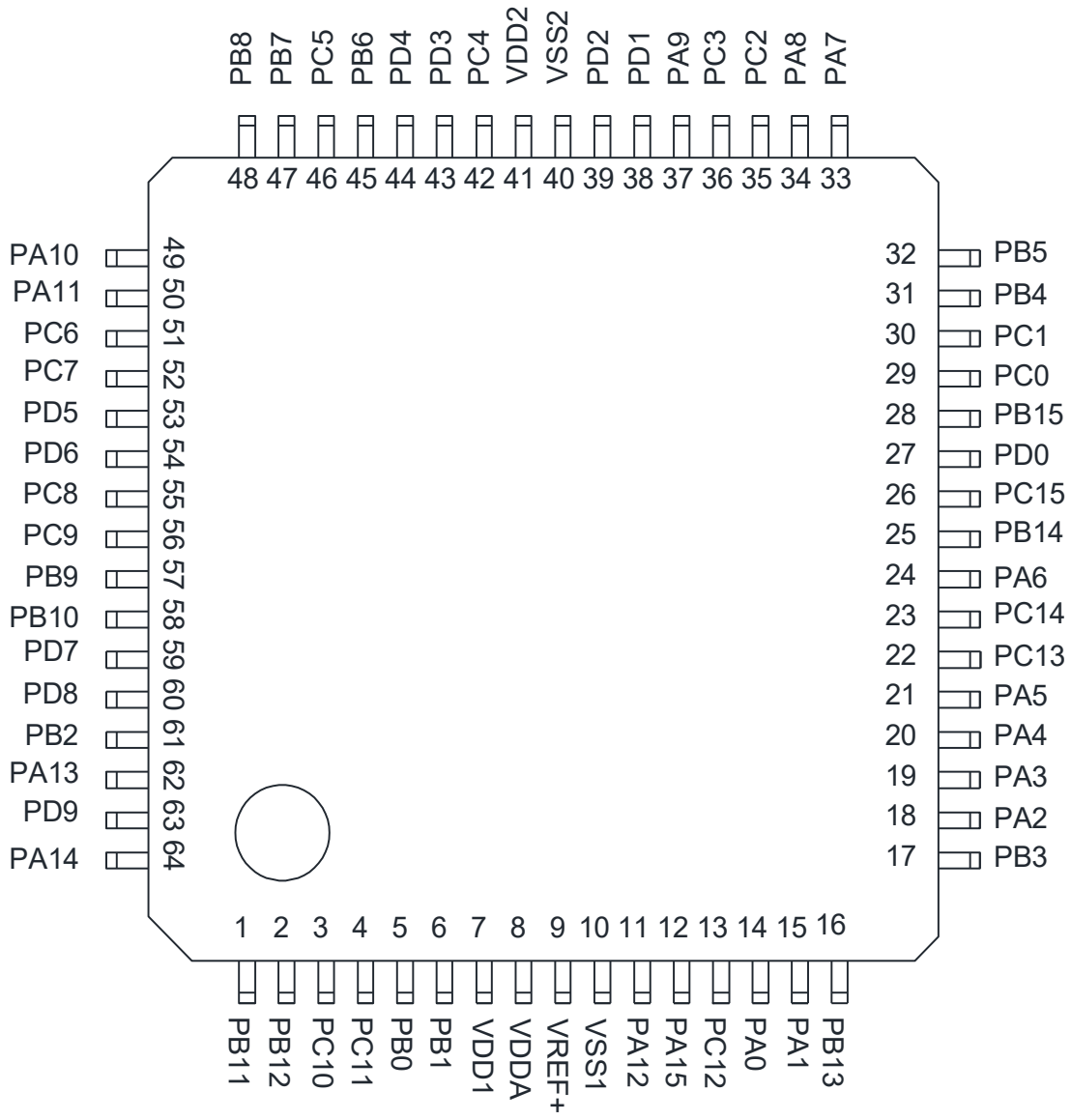

Figure 9-2 LQFP64 package